

2002

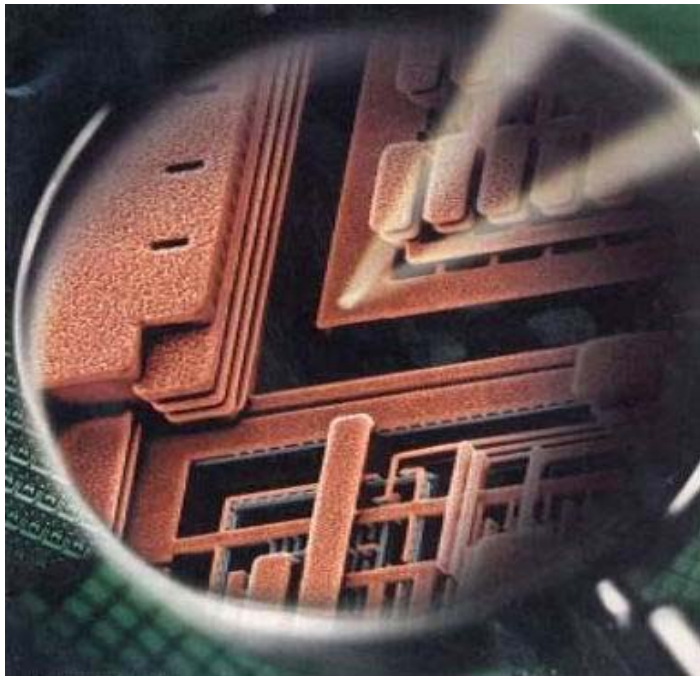
3

The 3rd KOREA TEST CONFERENCE



- : 2002 5 17 ()
- : ()

3



- ()
- A ()
- B (Built-In Self-Test)
- C ()
- D ()
- E (SOC)
- F ()

- : IC
- : IEEE Test Technology Technical Council
- : VeraTest, Davan Tech , Teradyne, Advantest Korea, Synopsys, Mentor Graphics, ASIC



?

3

가 5 17

SOC

SOC

가

가

Conference Chair

()

Program Chair

()

Program Co-Chair

()

Finance Chair

()

Finance Co-chair

()

Publicity Chair

()

Publicity Co-chair

()

Local Arrangement Chair

()

Program Committee

()

()

(Advantest Korea)

()

(LG)

()

(Mentor Graphics)

(Synopsys)

()

()

()

()

()

()

()

()

(Teradyne)

()

()

()

3

	A	B
09:00 ~ 10:00		
10:00 ~ 10:20	& (A)	
10:20 ~ 11:00	(1) (A)	
11:00 ~ 11:10		
11:10 ~ 11:50	(2) Dr. Kazuhiko Iijima (Davan Tech) (A)	
11:50 ~ 12:10	(3) (Teradyne) (A)	
12:10 ~ 13:30		
13:30 ~ 14:30	A (A)	B Built-In Self-Test (B)
14:30 ~ 14:40		
14:40 ~ 15:40	C (A)	D (B)
15:40 ~ 15:50		
15:50 ~ 16:50	E SOC (A)	F (B)



(1) : ()
Test Trend and Issues for Deep Sub-Micron Devices

(2) : Kazuhiko Iijima (Davan Tech)
Test Cost Reduction achieved with Embedded Test

(3) : (Teradyne)
High Speed/Resolution Converter Test Issue

()

5 17 () 13:30~14:30(A)

: ,

[A-1] Extended Burst - mode

, , (),
()

[A-2] CUT

, ()

[A-3]

, , ()

5 17 () 14:40~15:40(A)

: ,

[C-1] Boundary Scan PCB Fault Modeling
Fault Diagnosis

, ()

[C-2] ATE Test Pattern IC Junction
Temperature Control

, , , ,
()

[C-3] Verilog PLI PDP

, , ()

()

5 17 () 15:50~16:50(A)

SOC TEST

: ,

[E-1]

, , , ()

[E-2] SoC

, , , ,
()

[E-3] Test Decompression for SOC testing Using a
Variable Length LFSR

, ()

()

5 17 () 13:30~14:30(B)

Built-In Self-Test(BIST)

: ,

[B-1]

, , , ()

[B-2] Logic BIST

3-

DFT

(LG), , ()

[B-3]

, ()

()

5 17 () 15:50~16:50(B)

: ,

[F-1]

/ , , , , ()

[F-2]

, () , , ()

[F-3]

, , ()

5 17 () 14:40~15:40(B)

: ,

[D-1] A Neighborhood Bit-Line Sensitive

Faults Detection Algorithm For

Super High-Density Memories

, , ()

[D-2] Embedded DRAM BIST

, , ()

[D-3] March C-

, , , ()



◆Keynote Speakers

[]

Karlsruhe University

Bremen University

Bremen University

1997 ~

System LSI

CAE Center

Beam

10

20

15

5)

가

Dr. Kazuhiko Iijima

1980: BS from University of Tokyo, on Design Automation algorithms and systems

1982: MS from University of Tokyo, on Design Automation algorithms and systems

1982-1986: Research and teaching assistant in the faculty of engineering, University of Tokyo

1986: Ph.D. from University of Tokyo, on automatic placement and routing algorithms

1986-2000: Research and development, management positions in the Design Automation department in the General Purpose Computer Division, Hitachi, Ltd., Tokyo, Japan

Oct. 2000- : Director of Technical Services, LogicVision, Inc.

*

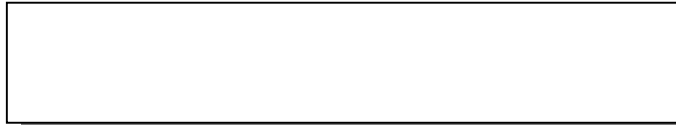
(<http://soc.yonsei.ac.kr/TEST>)

1983.2 :

~1997 :

~2000.5 : ST

~ : Teradyne Korea



가

<http://soc.yonsei.ac.kr/TEST/>

Registration

procedure

2002	5	10	:	1	,	3
2002	5	10	:	2	,	5

(: 126-

774644-13-001 :), fax(02-313-

8053) scan email(info@soc.yonsei.ac.kr)

가

02-2123-2775

가

TEL. (02)571-8100 FAX. (02)571-4929
 Add. 서울시 서소구 영재동 202번지
 E-mail. tenf@mail.yonsei.ac.kr

▶ Car
 경부고속도로 영재IC에서 5분 거리
 고속터미널에서 30분 거리
 김포공항에서 1시간 거리
 인천국제공항에서 1시간 40분거리

▶ Airplane
 삼성동 도심공항터미널 무료셔틀버스 운행
 (3시간 30분 간격으로 운행)
 - 호텔 -> 도심공항터미널
 오전 7:00 - 오후 6:30
 - 도심공항터미널 -> 호텔
 오전 7:30 - 오후 6:00

▶ Subway
 영재역 7번 출구 성남빌딩
 ● 무료셔틀버스 이용: 서소구인혁관 앞
 -> 셔틀버스 이용: 관승주차장앞 07-20번

Design-for-Test 가
Soc

VeraTest

RTL - to - Layout

Timing - Closure
Signal Integrity

One - Pass

㈜베라테스트

Info@veratest.com

www.veratest.com

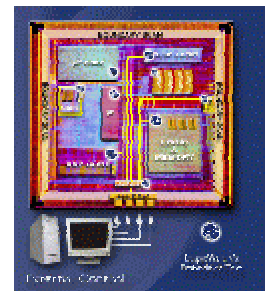
LogicVision's Comprehensive SOLUTION

Our Embedded Test technology reduces the challenges of developing and testing complex semiconductors by solving test and diagnostic challenges at every stage of semiconductor design, production, and application use. As complex chips are incorporated into boards, systems, and end products, your downstream customers can benefit from the Embedded Test solutions integrated in the devices to assist in the development, diagnosis, and test of their products. Once deployed in the field, LogicVision's Embedded Test solution enables system self-test and debug at installation and allows for the repeated field test of the system components throughout product deployment.



Embedded Test Solutions

LogicVision's Embedded Test delivers a comprehensive intellectual property test solution addressing chip design, chip manufacturing, system level testing, and ongoing test and diagnosis of the final products.



DAVAN
DAVAN TECH CO., LTD.

311, Seonun Tower Bldg.
201-1, Seongnam-myeon, Gyeonggi-do
Suwon, Korea 146-821
Tel : +82-2-471-0028

LogicVision



TERADYNE

Catalyst

Defining
System Silicon
Test

THE CATALYST FAMILY

Tiger

The Catalyst Family

© 2004 Teradyne, Inc. All rights reserved.

The more **complex**
your IC design

the **simpler**
your choice.

Synopsys Korea, Ltd.
19th Fl., Hanso Bldg. 798-1
Yousong-dong, Kijung-gu
Seoul 152-881, Korea
Tel: 82-2-551-8100
Fax: 82-2-558-2108

<http://asiapac.synopsys.com/korea/korea.html>

SYNOPSYS

SYNTEST
The Testability Category

TurboBIST-Logic for:

- At-speed self testing of ASICs/SOCs with multiple clock domains
- Reduced ATE costs
- ★ In-field remote testing or non-invasive testing
- Reduced Time-to-Market

Offers Boundary Scan Synthesis, Memory-BIST, Logic-BIST, Scan Synthesis, ATPG, DFT Checkers, Fault Simulation, Debug and Diagnosis

SynTest Korea, Ltd.
Tel: (0)2-561-7824 e-mail: jjpark@syntest.com
<http://www.syntest.com>

ADVANTEST®
Advantest Korea Co., Ltd.

Compression.
Squeeze your scan test data down to one-tenth its size.

Design-for-Test

TestKompress™
more information: <http://www.mentor.com/dft>

Mentor
www.mentor.com

ASIC

<http://asic.yonsei.ac.kr/>

: VeraTest
Davan Tech
Teradyne
Advantest Korea
Synopsys
Mentor Graphics

ASIC

System IC Testing

Technology Group

IC

<http://soc.yonsei.ac.kr/SystemIC/>