



An Industry Perspective on Current Embedded Test Adoption

Agenda

- An Integrated Scalable Solution
- Real Cases of Success
- Measuring Against Objectives
- What were the Challenges?
- How to Overcome the Challenges!
- In Conclusion

LogicVision's Solution

Design



Silicon Debug



Manufacturing

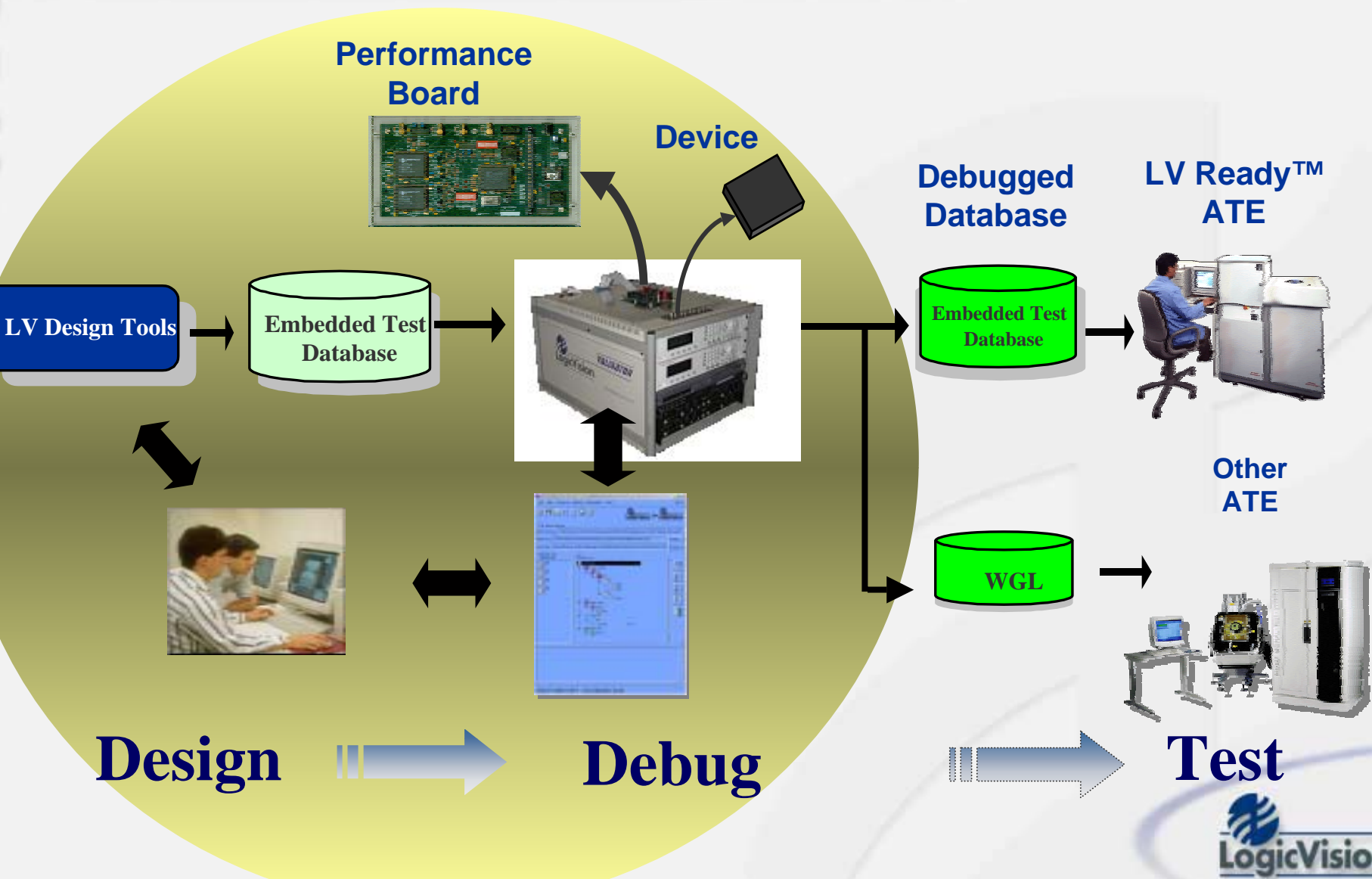


Board/System Test



Embedded test and diagnostics
Single unified data base
Integrated flow
Scalability

Integrated Test and Debug Flow



National Ethernet Physical Layer IC

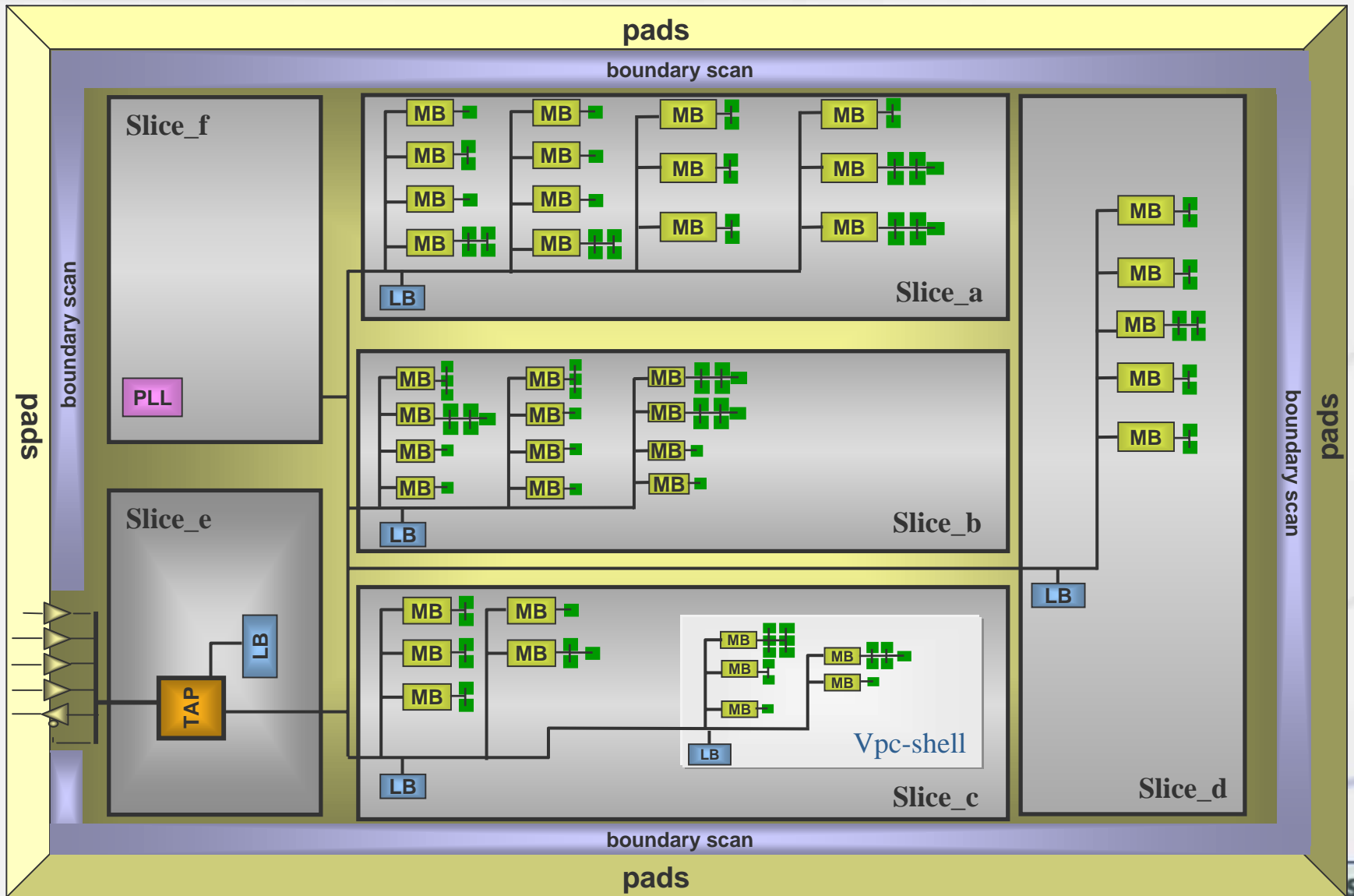
- DP83865 Transceiver
 - ◆ >1M gates of logic
 - ◆ 10 Mbits of RAM
 - ◆ 9 embedded cores
- Utilizes LogicVision's logic BIST
- LogicVision ETA software located an at-speed logic design problem in < 1 day



Oak Technology's TL950 Chip – HDTV System On a Chip

- 8 million gates
- 98 memories
- 7 layout regions/cores
- Frequencies from 266MHz up to 300MHz

Oak TL950 BIST Architecture



Broadcom Ethernet Switch

- Scalable 12 port multi-layer gigabit switch
 - ◆ 10M gates
 - ◆ 88 RAMs
 - ◆ Multiple cores
 - ◆ Clock domains operating up to 156 MHz
- Utilizes LogicVision's hierarchical test
 - ◆ 15 ELT blocks, 13 designed for logic BIST at 125 MHz
 - ◆ Top level logic BIST designed for 40 MHz operation

Trebia Networks

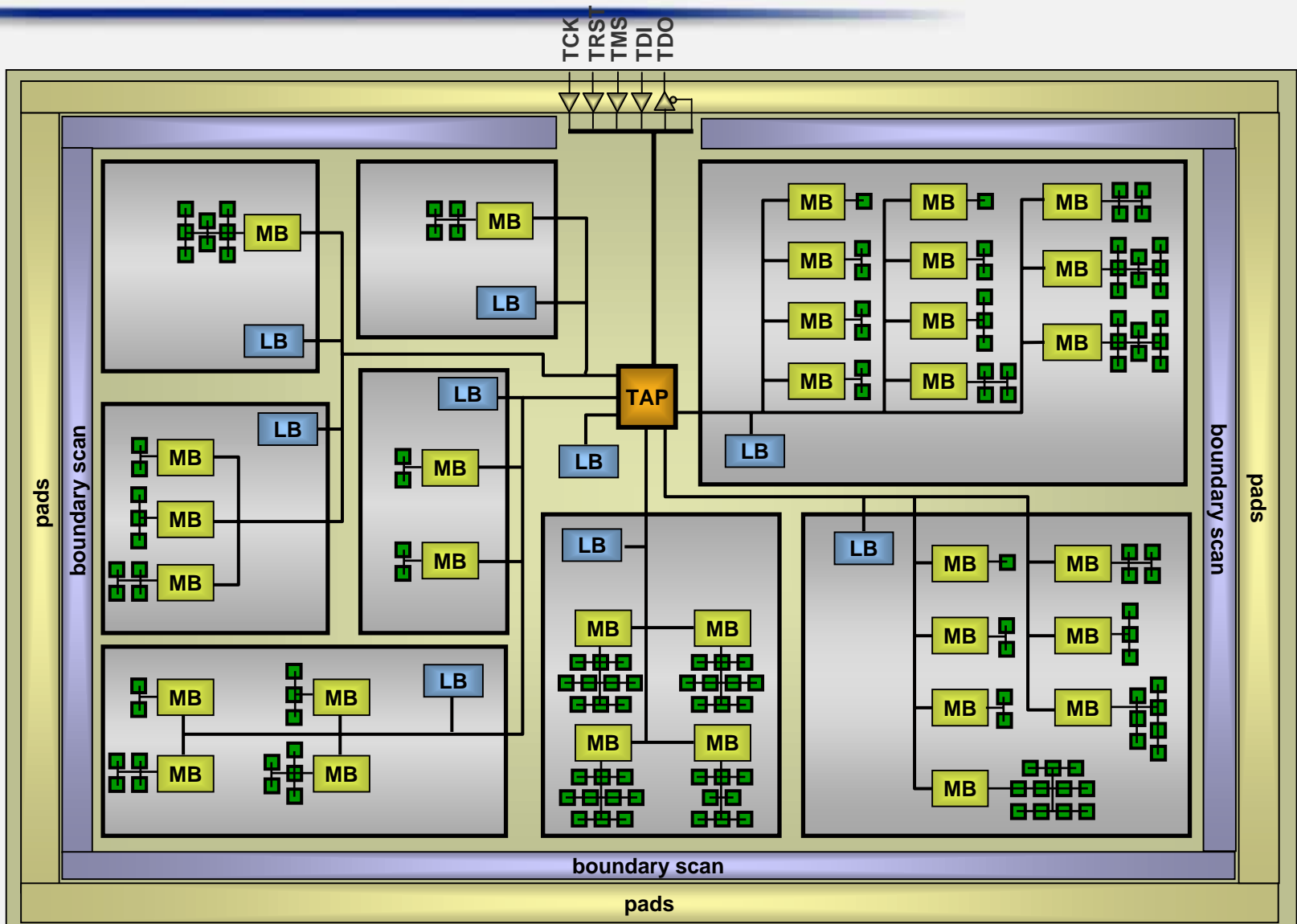
Trebia Networks SNP chip – Storage network processor

- 86 million transistors
- 116 memories (10 Mbits)
- 9 embedded cores
- 3 clock frequencies

Device debug completed in
3 days



Trebia SNP Test Architecture



Agere TSOT1610

**STS-192/STM-64 SONET/SDH
Path Processor & Terminator**

Technology: (0.14 μ m CMOS)

Package: High Density Flip Chip,
1724 balls

Interfaces: 2 @ SFI-4,

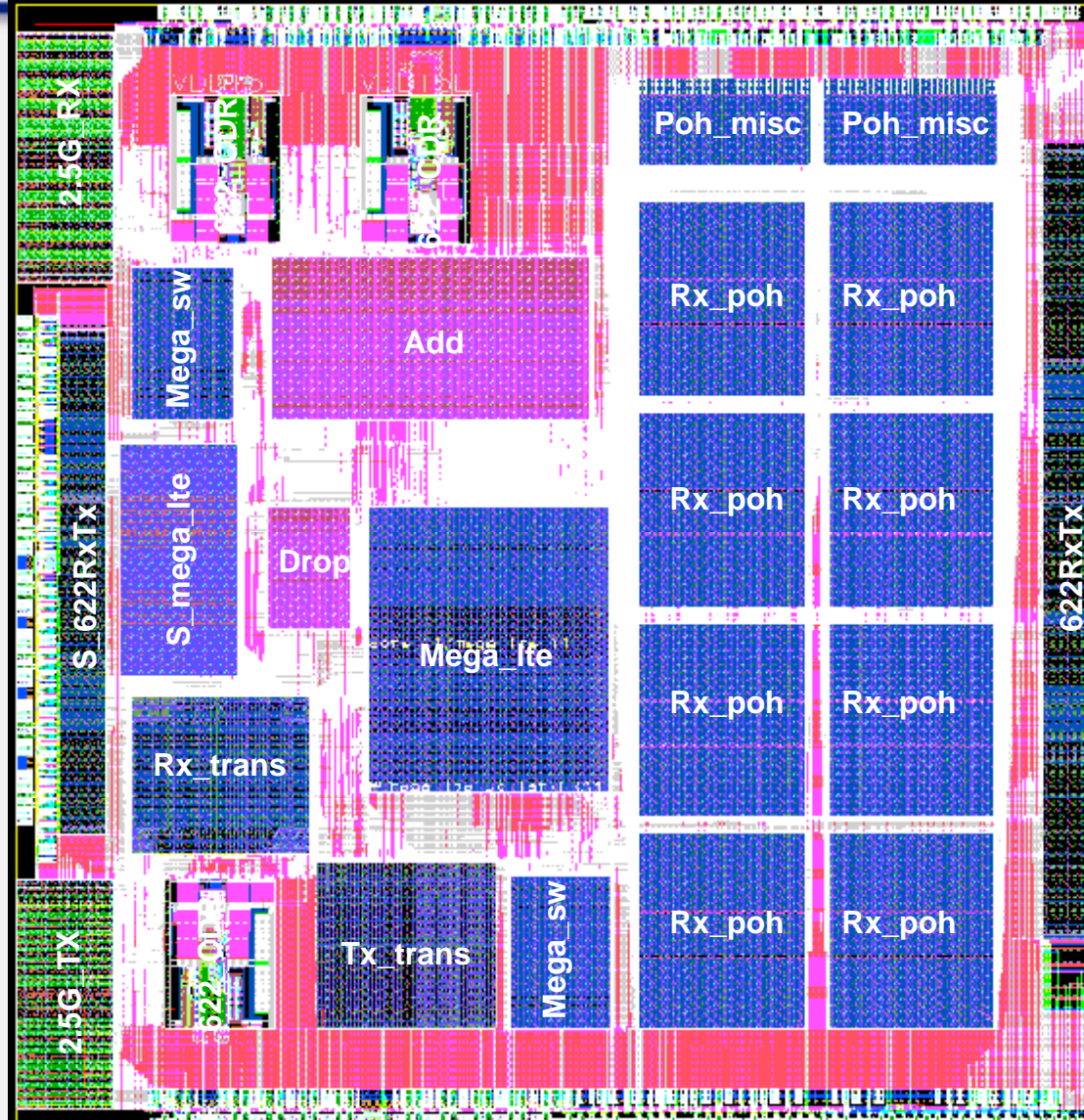
2 @ STM backplane 622MHz

2 @ STM backplane 2.5 GHz

Total Gates: ~11 Million

Total Memory: ~400Kbits

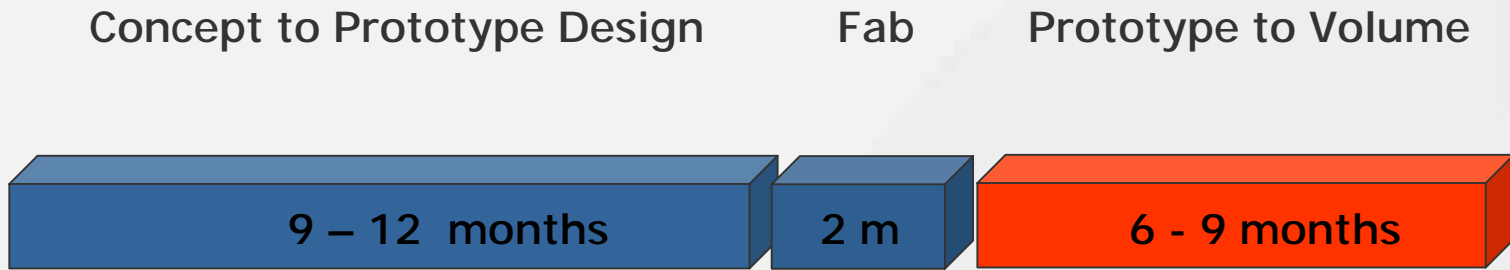
Clock Nets: ~3400 (top level),
~200 clock domains




General Industry Objectives

- To achieve a significant **Reduction in Test Costs**, while:
 - ◆ Improving **TTM** (Time-to-Market),
 - ◆ Improving **TTV** (Time-to-Volume).
 - ◆ Improving **Quality**.
 - ◆ Providing **Scalable** and **Effective** test methods
 - ◆ Infrastructure for **Re-use** of test **In System** and **In Field**
- Reduce projected capital investment in ATE
 - ◆ Enable **PC Based** testing
 - ◆ Increase **Throughput** and **Yield**

IC Time-to-Market Reality




**Need to reduce
Debug Times!**

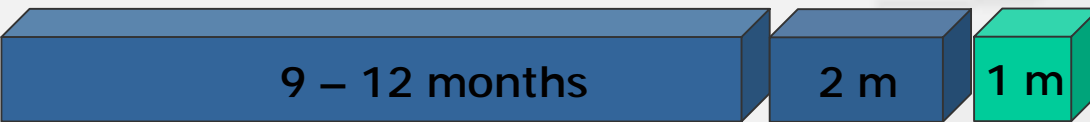
Source: Gartner Dataquest 2002

TTM Improvements with Embedded Test

Concept to Prototype Design

Fab

Prototype to Volume



SNP Design debugged in just 3 days!

“With LogicVision’s embedded test methodology, we were able to perform root cause diagnostics to failing gates in a matter of minutes on the LV Ready Teradyne Catalyst .

The combination of the embedded test hardware and embedded test access software allows National to remain competitive with time-to-market including root cause diagnostics.

LogicVision’s embedded test solution is fast becoming a key component for National.”

Larry Whitcomb, Director of Test Development.

Oak Technology's Quote



“The unique combination of LogicVision's Embedded Test technology and the Validator enables us to perform at-speed debug of our multi-million gate chips in days instead of weeks and pinpoint manufacturing yield hazards for rapid analysis and corrective action. We believe this fast, advanced debug capability will help us maintain a leading edge in the market by delivering robust, highly complex devices to our customers in a timely manner.”

Alex Sinar
VP Operations
Oak Technology, TeraLogic Group





With LogicVision's embedded test, we had the Draco chip up and running within 45 minutes of receiving first silicon.

This is unprecedented within Broadcom for this complexity of a device. Broadcom sees the embedded test methodology as a key component for high quality at-speed test that also enables rapid bring up of first time silicon, even for the most complex of devices.

This combined with the diagnostic capabilities make embedded test essential in moving forward.

*Martin Lund
Product Line Manager,
Switching Products*

"While designing a complex, hierarchical chip (an 86 million transistor Storage Network Processor chip), we looked for a test methodology that not only met our test needs, but also provided key customer benefits as well. Using LogicVision's Embedded Test technology allows us to deliver accelerated time-to-market and enhanced diagnostics and debug capabilities to our customers."

*Wayne Koch, Vice President,
Hardware Engineering*

LogicVision's Logic BIST on TSOT1610



- Investment: marginal increase over traditional scan
 - ◆ +2% die-size
 - ◆ +5% logic transistors
- And significantly more complex design
 - ◆ Increased number of clock domains by 2x-3x
 - ◆ Additional resources for architectural planning, verification and analysis (1 dedicated headcount)
 - ◆ **Most** of the effort could be dry run in parallel with completion of the logic design
 - ☞ Depending on the willingness of the design team to make it work, trade deterministic design time for unpredictable post silicon ATE debug

LogicVision Validator on TSOT1610



- TSOT16 is a 11 million gate design, we put working prototypes in the hands of our application engineers in 30 minutes!
- As pre-screener increased ATE proto yield from <10%, to >50% (cut'n'go devices)
- Dramatic reduction in test development/debug effort
 - ◆ Devices debugged on ATE were of known quality, allowing the test engineering focus on the test program
- Low cost, desktop-based platform (\$150K) compared to ATE (\$2M-\$6M)
- Substantially reduces requirements on ATE test time for shipping of initial prototype devices, and debug and analysis of returned devices.

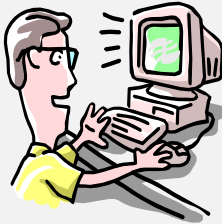
Challenges to Adoption

- ◆ Organizational structure (resources & processes)
 - ☞ Barrier between Design-DFT-Manufacturing
- ◆ Develop new skill sets
 - ☞ Designers must become DFT aware
- ◆ Added overhead to area and design cycle
 - ☞ Must be balanced with savings in manufacturing
- ◆ Integration into existing design flows/methodologies
- ◆ Integration into manufacturing

Organizational Paradox

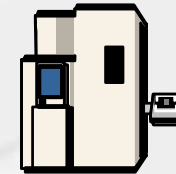
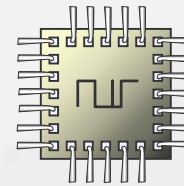
Design Test Management

“It is really not my problem, but I will do what I can to help out.”



Manufacturing Test Management

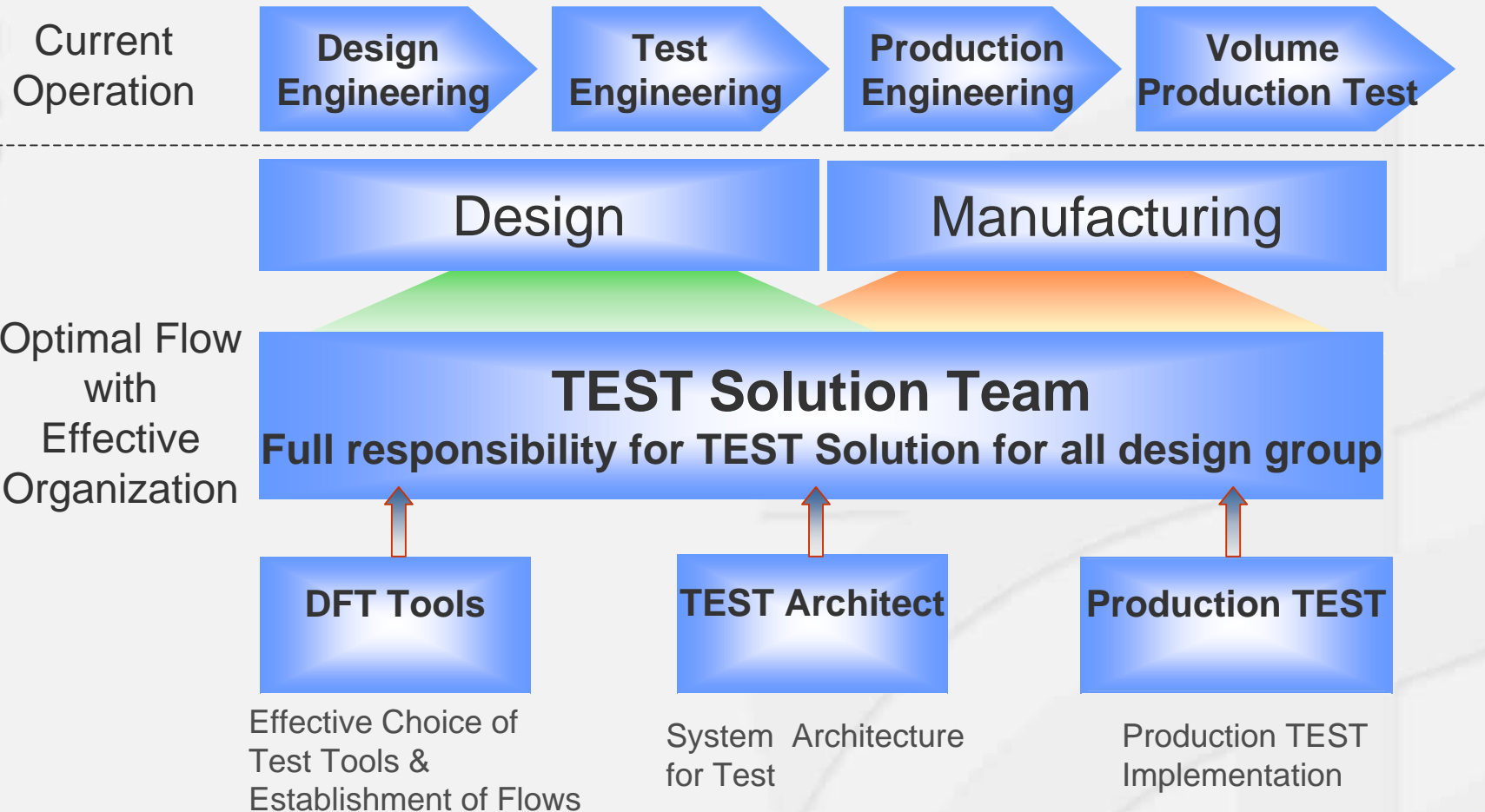
“I have little control on the design process! I will buy the best testers possible and perform as much testing as possible to ensure the expected quality.”



Solutions to the Challenges

- ◆ Organize to give organizations visibility to full flow from design to manufacturing
- ◆ Provide extensive training on new methodologies
- ◆ Work closely with design/DFT teams to establish the proper flows for embedded test
- ◆ Work with manufacturing teams to streamline handoff from design to manufacturing

Organizational Challenges/Solutions



TEST is an Integral Part of Design for SOC

Engineering Objectives to Live By (1)

- Automate routine, tractable problems
 - ◆ In this case: integrated logic BIST, memory BIST, & JTAG
 - ☞ At speed, with fault isolation, no vectors, and very pin multiplex friendly
 - ◆ Just get on with it
 - ☞ Feels like the early days of logic synthesis...
 - To be vector-less, it must be HW the CAD tool recognizes, not exactly your way
 - ☞ Focus on making it work, not elevating minor bugs or omissions to show stoppers
 - ◆ These are tough times!
 - ☞ Few products are so good the market will wait, accept lower quality, and higher prices
 - ☞ This technology does not expedite time to tape out, making the roll out harder
 - ☞ TIME TO MONEY!

Engineering Objectives to Live By (2)

- Don't wait for the perfect solution and use that as an excuse to pass by (1)
- Focus test engineering on the problems that don't easily automate
 - ◆ Analog, Parametric IO (SERDES!)
 - ☞ the big \$'s are in large numbers fast digital pins
 - not AWG's & digitizers
 - ☞ Jitter margin, Sensitivity, Linearity, BER, output impedance, rise/fall time, VOH/VOL...
 - ◆ High speed circuits where BIST must be part of the functional architecture
 - ◆ The escapes that need to be functionally reproduced and screened in production test (even some hope here for ATE manufacturers :~)
 - ☞ Not random faults
 - For example, my nightmare, repeatable resistive vias between at speed logic BIST domains
 - ☞ 50 DPPM will never be a slam dunk

Concluding Remarks

- It is up to us to rally around good solutions and drive them to profitable critical mass
- ***It will be the design flow integration, not the nuances of the BIST algorithm, that will make vector-less, at speed test, ubiquitous***
 - ◆ And through this we can contribute to digging our industry out of the worst down turn of its history