Advanced ADC BIST Based on Histogram Testing

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Abstract
A scheme of histogram-based ADC (Analog to Digital Converter) BIST (Built-In Self-Test) reducing the testing time and hardware overhead is presented. In this paper, the main characterization parameters of ADC such as offset, gain and non-linearities are derived and analyzed. The proposed BIST uses ramp signal as input signal in order to minimize the BIST hardware. As a response analyzer, 2 counters are used to calculate static parameters for ADC. The practical implementation is described and the performance is evaluated. It is shown that the proposed method makes the hardware overhead and testing time reduced.

I. Introduction
ADC is one of the most frequently used mixed-signal blocks in a SoC (System on a Chip). As SoC usually includes ADC, testing ADC has become the important issue. The inaccessibility of ADC in a SoC turns the testing into a more challenging task. The required test cost of ADC drastically increases because the ADC testing usually requires high quality ATE (Automatic Test Equipment). For these reasons, BIST techniques for the ADC testing which can alleviate test cost and provide accessibility have been proposed.

Various BIST schemes have been developed. [1][2][3][4] One of the most popular techniques used for the testing of ADC is the histogram BIST. [1][2] It is based on a statistical analysis of how many times each digital code appears on the ADC output in order to determine the ADC characteristic parameters. This technique is widely used for its precision, however, it needs huge amount of additional circuitry and testing time to achieve statistically satisfactory results. The time decomposition scheme which reuses hardware resources by calculating ADC parameters sequentially to minimize the extra on-chip hardware is proposed in [1]. In terms of the testing time, however, testing each static parameter sequentially increases the testing time 4 times. In [2], schemes of BIST reducing the testing time are presented but hardware overhead increases about 4 times. While previous works reduce just one of the testing time or hardware overhead, the advanced ADC BIST method reduces both of them. This method is proposed in this paper.

II. Proposed ADC BIST scheme and implementation
The test stimulus as an input test signal of ADCs is a ramp signal. Figure 1 describes the test stimulus and the histogram generation for a 4-bit ADC when the test stimulus is applied.

Min/Max is the minimum/maximum value of the test signal. The ramp stimulus covers the entire ADC input range FS (Full Scale). So, it does not cause clipping. The advantage of the ramp stimulus is that the ideal number of bins per each code bin is constant for all codes.

Figure 1 Test stimulus and its histogram

Histograms support the analysis of the ADCs static performance parameters such as offset, gain, DNL (Differential Non-linearity) and INL (Integral Non-linearity). Some histograms of typical functional failures are illustrated for ramp input stimuli in Figure 2.

Figure 2 Transfer curves and histogram of functional failures
Since the offset causes a shift in the analog to digital code transfer curve, the offset can be expressed as the difference between the count of '0' and '2^n-1':

\[
Offset = \frac{(H(2^n - 1) - H(0)) \times 2^n}{N_t},
\]

where \(N_t\) is the total count number for all codes, \(n\) is the resolution of ADC, and \(H(i)\) is the code count number for the \(i\)th code. The offset can be simply expressed using the relation:

\[
H(0) + H(2^n - 1) = 2H_{ideal}
\]

where \(H_{ideal}\) is the ideal code count number for each code:

\[
Offset = \frac{2(H(0) - H_{ideal})}{H_{ideal}}
\]

The gain error is defined as the difference between the ADC's transfer curve slope and the ideal slope. The gain error which
results in a change in average code count can be expressed as follows:

\[ \text{Gain} = \frac{\sum_{i=1}^{N} (H_i - H_{\text{ideal}})}{\sum_{i=1}^{N} H_i} \]

Assuming that the ADC is faultless, the gain value would be 1. In this case, the following expression would be 0.

\[ \sum_{i=1}^{N} (H_i - H_{\text{ideal}}) = 0 \]

The DNL error is defined as the difference between the measured code counts and the ideal code counts. The INL error is defined as the integration of the DNL. DNL and INL can be expressed as follows:

\[ \text{DNL} = \sum_{i=1}^{N} (H_i - H_{\text{ideal}}), \quad \text{INL} = \sum_{i=1}^{N} (H_i - H_{\text{ideal}}) \]

Therefore, all static parameters of ADC are related to \( H(i)-H_{\text{ideal}} \) or \( \sum (H(i)-H_{\text{ideal}}) \). If there is no fault in ADC, \( H(i)-H_{\text{ideal}} \) and \( \sum (H(i)-H_{\text{ideal}}) \) would be nearly 0.

In order to calculate \( H(i)-H_{\text{ideal}} \) or \( \sum (H(i)-H_{\text{ideal}}) \), the BIST architecture which mainly consists of two counters is proposed.

![Figure 3 Proposed BIST architecture](image)

The overall BIST architecture for the ADC BIST scheme is depicted in Figure 3. It consists of the ramp signal generator, transition detector, 2 counters and comparators.

During test mode, the test stimulus of the ramp signal is applied to the ADC through the analog MUX. The test stimulus will be converted into a binary code at the sample frequency of the ADC. The transition detector monitors the LSB of the binary code to detect a transition in ADC output. The counter starts counting when the testing starts. The content represents the code counts. When a transition is detected the content of the counter \( H(i) \) is compared with reference value \( H_{\text{ideal}} \) determined by the offset or DNL specifications of the ADC. Once the content is checked, a pass/fail decision is made for offset and DNL errors, and the counter is reset for next code counts measurement.

The gain and INL are determined by successively adding the \( H(i)-H_{\text{ideal}} \) from the first code, up to the code for which the INL is determined. To calculate \( \sum (H(i)-H_{\text{ideal}}) \), the down counter is used. When the test begins or the output code is changed, the MSB of the down counter is set to '1', where '10...00' is equal to \( H_{\text{ideal}} \). \( H_{\text{ideal}} \) can be adjusted by changing the slope of the input ramp. During the test the down counter counts down. If a transition is occurred, the content of the down counter contains the value of \( \sum (H(i)-H_{\text{ideal}}) \). The contents are compared with the reference value (almost zero) given by the gain and INL specifications of the ADC.

When the input ramp signal reached to \( V_{\text{max}} \), the EOT (End of Test) signal is generated by the comparator.

III. Experimental results

In order to validate the proposed BIST structure, its performance is evaluated. An 8-bit flash ADC is used as a CUT (Circuit under Test). To create each type of errors, ADCs that have an open or a short fault in the comparator or some variations in resistances are generated. The proposed BIST circuitry is verified by simulation with 64 test circuits. As a result of simulation, the proposed BIST can detect each type of errors (offset, gain, DNL and INL).

Table 1 shows a comparison between previous works and the proposed BIST in hardware overhead and test length. The proposed BIST consists of two counters without ALU and memories, and needs only 1 test phase.

<table>
<thead>
<tr>
<th>Table 1 Hardware overhead and test length comparison</th>
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<tbody>
<tr>
<td>Hardware overhead</td>
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<td>Medium (Comparators, RAM or Counter, Registers, Adder, Fine decimator, FSM in control phase)</td>
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<tr>
<td>Large</td>
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<td>Testing time</td>
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The results show that both the hardware overhead and test length are reduced while achieving an efficient detection of static fault in proposed BIST compared with previous works.

IV. Conclusion

An advanced ADC BIST, which is based on histogram method, is proposed. Analyzing static parameters such as offset, gain and NL, good estimates of static parameters can be obtained. The ramp signal as a test stimulus and two counters as a response analyzer are used, so the BIST has reduced the amount of additional on-chip circuitry. Moreover, only one test period is needed to test ADC, so the testing time also decreases. Experiments conducted on various faulty converters have validated the BIST since the proposed BIST can detect each type of static faults.

References