Efficient BIST scheme for A/D converters

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Abstract: As SOC and complex systems usually include analogue IPs, it becomes more important to test analogue devices efficiently. The reason for this is that analogue testing for high quality requires substantial testing costs although the analogue portion in a whole chip or in a system is usually very small. In the paper, an efficient low-cost built-in self-test (BIST) scheme is developed for testing A/D converters. The key ideas are to use a triangular wave as a test input signal and to analyse the output response for functional testing. In order to perform functional testing, new fault models called successive value, oscillation and bit faults are proposed. Testing these faults guarantees the quality of A/D converters. For experimental results, a Δ–Σ A/D converter and a pipeline A/D converter are used. The results show that the new BIST scheme is very efficient in terms of fault coverage and hardware overhead.

1 Introduction

The increasing complexity of circuits creates increases in testing difficulties as well as testing costs. Today, for VLSI systems, manufacturing cost is dominated by the cost of testing. Testing has a significant impact on both the quality and cost of a product. For mixed signal systems that integrate both analogue and digital functional blocks onto a single chip, testing the analogue part has become a bottleneck, because digital testing has become quite mature, but analogue testing has not. Thus the testing of analogue circuits is very time consuming and expensive compared to testing digital circuits. A/D converters are commonly used analogue devices in most ICs. Testing methods for A/D converters have been developed. Since an automatic test equipment (ATE) based approach is expensive, BIST, in which both stimulus generation and response analysis are performed on-chip, is receiving increased attentions [1]. Since at-speed test is available and requirements on the external test equipment are less stringent under a BIST approach, BIST is gaining popularity as an effective solution testing in terms of cost and quality, despite its hardware overhead. Within the past few years, most of the proposed BIST techniques used for testing A/D converters use digital signal processing (DSP) capabilities [2, 3]. The BIST scheme, using DSP capabilities, calculates the characteristic parameters of converters such as SNR, frequency response, harmonic distortion and intermodulation distortion. This approach is a practical method for a pass/fail decision because it can be done in the digital domain. However, the technique needs a D/A converter and DSP resource (such as a DSP core) on the same chip, as well as intensive computation to compute the characteristic parameters of converters. In addition, the D/A converter must be a Δ–Σ A/D converter. The viability of this technique depends on a number of requirements, such as the presence of pre-existing DSP capabilities and the presence of both an A/D converter and a D/A converter. Another BIST approach uses pulse response sampling [4]. This BIST uses pulse trains of varying duty ratio, generated from a digital linear feedback shift register (LFSR), as a test stimulus. The responses of the device under test (DUT) are sampled and compared with reference voltages to generate binary sequences that can be compressed to yield a signature for the anticipated responses. The BIST scheme using pulse response sampling has the advantage of a very small hardware overhead, but it takes a long time to test in high fault conditions. Finally, the BIST architecture, which is most widely known, is a histogram-based analogue BIST architecture [5–7]. This method is based on statistical analysis of the A/D converter output code. In this approach, an analogue signal is applied to the A/D converter input and the number of times each code appears on the A/D converter output is recorded. These recorded samples are compared with theoretical values and then the BIST makes a decision whether the A/D converter is fault-free or faulty. To store both the measured and ideal histograms, the histogram test technique requires a large amount of hardware resources both in terms of memory and operative resources. In addition, a large number of samples and several successive periods of the signal are required to achieve satisfactory results.

This paper investigates the viability of a new BIST approach. The input test signal waveform of A/D converters is a triangular wave obtained from an integrator. Then the output of the A/D converters is compared with the reference voltages, which are related to the three defined fault models used by the BIST. The proposed scheme is applicable to any A/D converter because it is related to functional testing. Comparing this new BIST with other BIST, this scheme does not need any DSP resources. Moreover, the proposed BIST has a small hardware overhead but achieves high fault coverage. Just three periods of input signal are required to achieve high fault coverage, so test time is reduced.

2 New test methodology

Common BIST circuitry used for testing A/D converters involves applying a sinusoidal signal or a ramp signal as a

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test stimulus to associated converters. Using a sinusoidal wave, it is easy to generate and perform a frequency domain test for converters, but DSP resources are required to analyse the output code of the A/D converter in the frequency domain and testing takes a long time, because of complex computations such as FFT. Another commonly used test stimulus is a ramp signal whose generator is simply designed. However, the BIST using a ramp signal as a test stimulus requires a very precise and linear ramp signal generator to test the components correctly, and it cannot be used for a decreasing code test.

The test stimulus of the proposed BIST is a triangular wave depicted in Fig. 1*a*. Applying the triangular wave, we compensate for using a sinusoidal signal or a ramp signal. Using the triangular wave as the test stimulus makes it easy to analyse the circuit in the time domain so that the testing time is reduced, and all decreasing code transition tests are also available. However, the ideal analogue signal shown in Fig. 1*a* is difficult to generate, so the modulated triangular wave presented in Fig. 1*b* is used as the test stimulus and the modulated signal is actually obtained from the triangular wave generator. The output of the DUT is also a triangular wave in the digital domain if the A/D converter under test is fault-free. This scenario is shown in Fig. 1*c*. The output signal is differentiated to efficiently analyse the circuit using the BIST. The differentiated signal is the rectangular pulse train depicted in Fig. 1*d*.

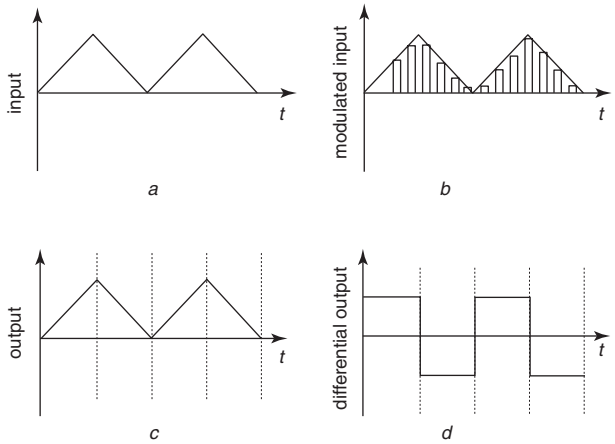

Fig. 1 *Test stimulus and output of A/D converter, and differential output values*

The practical model looks as in Fig. 2, which shows the differential output values of a fault-free A/D converter. T_p is the time band of the positive differential output values of the A/D converter and T_n is the time band of the negative component. The normal value is the range of slopes that the triangular wave could obtain.

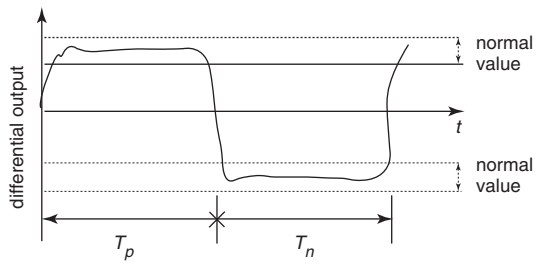

Fig. 2 *Differential output values of fault-free A/D converter*

The BIST observes the differential output values of the DUT to analyse the A/D converter. Then, the BIST classifies the DUT as fault-free if all specifications are satisfied. Otherwise, the BIST classifies it as faulty. We define the new fault models as successive value (SV), oscillation (OSC) and bit faults, and these models are shown in Fig. 3.

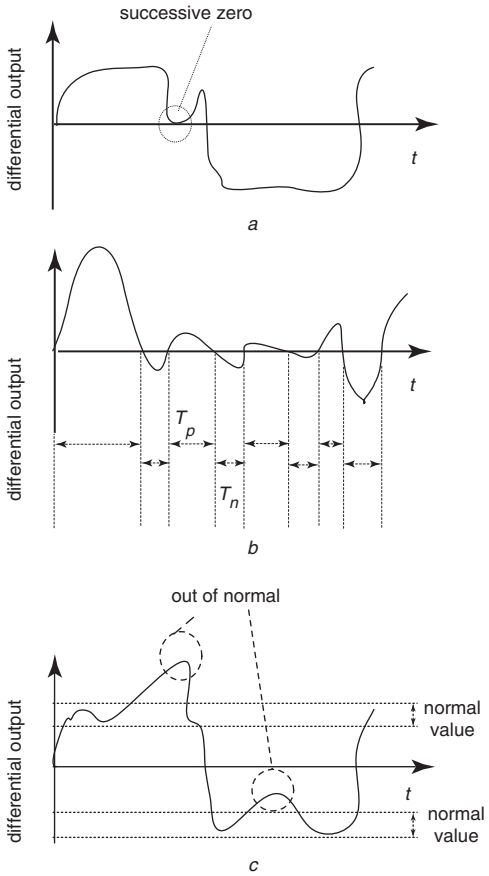

Fig. 3 *Fault modelling*

A SV fault is detected when successive 0 s appear in the differential output values. The numerical simulations show that three successive 0 s are suitable to classify the DUT as a faulty device.

An OSC fault is detected when the difference between T_p and T_n is greater than the threshold or when a change of sign occurs several times in a specified short period of time. For an ideal triangular wave, T_p and T_n should have the same value, and the change of sign should happen just once during one complete cycle of the triangular wave. Through several simulations, the BIST classifies the DUT as a faulty device when the difference between T_p and T_n is greater than 3.

A bit fault is detected when the differential output value exceeds the 'normal value'. Since the triangular wave has a fixed slope, the differential output values should be the same. We derive the tolerance range to give a 'normal value' to minimise the percentage of misclassifications.

Using the three defined fault models, the BIST analyses the DUT. It has been proven by simulation that the fault models are sufficient to classify the DUT as either fault-free or faulty. Simulations also show that the BIST circuit effectively detects not only the catastrophic faults, but also some parametric faults.

A gain error and an offset error are defined in Fig. 4. D_{ideal} is the ideal A/D converter output code and D_{out} is the

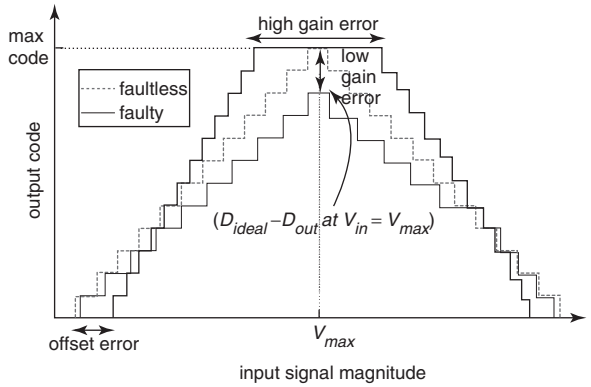

Fig. 4 *Gain error and offset error*

practical A/D converter output code. The gain error is defined by the difference between the A/D converter's transfer curve slope and the ideal slope. If there is a gain error in the A/D converter, the proposed BIST detects it as a bit fault because the differential output values would be different as a result of slower changes or faster changes in the A/D converter output. The offset error is defined by the difference between the first measured code width and the ideal code width. Offset errors can be detected because successive 0 s will appear in the differential output values. The proposed BIST detect thus as a SV fault. The proposed BIST circuit thus effectively detects some parametric faults.

3 BIST implementation

The overall architecture for the A/D converters BIST scheme is depicted in Fig. 5. It consists of a triangular wave generator, a BIST controller, a differentiator, and fault detectors.

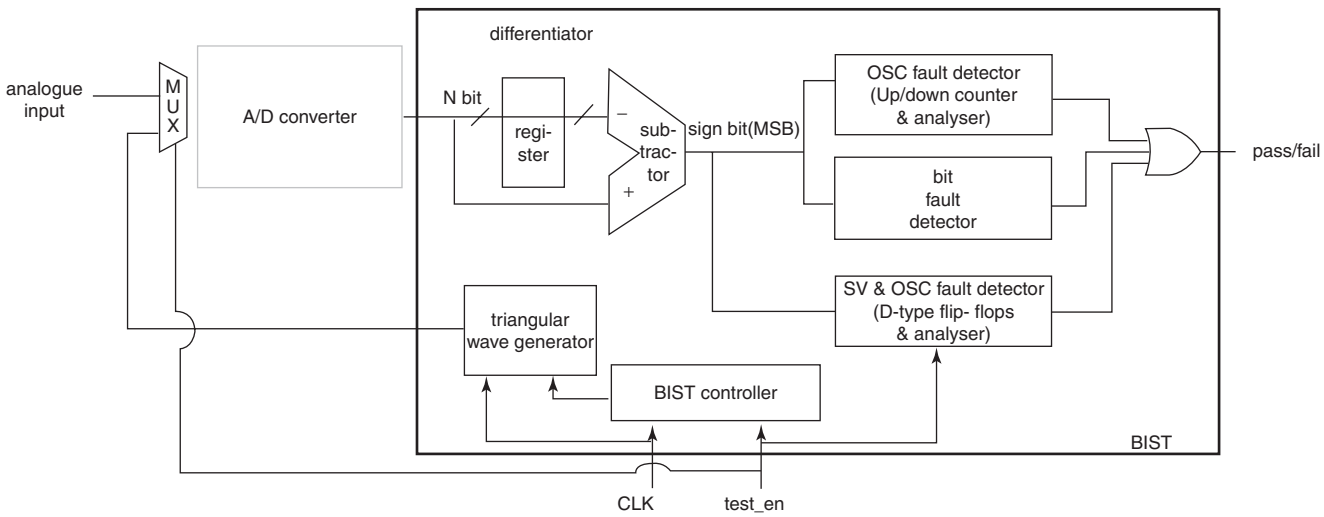

Fig. 5 *BIST architecture*

The BIST requires a triangular wave generator to generate the test stimulus, a register to store the digital output temporarily, a subtractor to obtain the difference between adjacent output values of the A/D converter, a counter to obtain the differential value between T_p and T_n, and detectors to detect the three defined fault models. We can conclude that the proposed BIST requires only a small hardware overhead. The analogue is a test signal generated by the triangular wave generator is input to the A/D converter through the MUX during testing, and the BIST analyses the digital output from the A/D converter. The output is differentiated and then the fault detectors make the pass/fail decision after response analysis. The BIST controller controls the other functional blocks to detect faults efficiently.

The test stimulus generator is shown in Fig. 6. The triangular wave is obtained using a clock. The clock of the A/D converter is inserted into the demultiplier to acquire the desired clock which is then integrated using switched capacitors to acquire the triangular wave. Finally, a sinusoidal wave is multiplied to obtain a modulated signal.

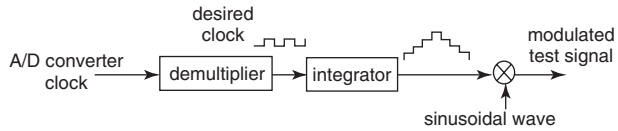

Fig. 6 *Test stimulus generator*

The differentiator is shown in Fig. 7. Because the slope of the triangular wave is fixed, the difference between adjacent output values of the DUT is also fixed if the DUT is fault-free. The differentiator samples the output values of the DUT and stores the value using a D-type flip-flop. The difference between the current value and the stored value is obtained from the subtractor. This represents the differential output value of the DUT.

The counter is used to detect OSC faults. The counter operates as an up-counter or as a down-counter when the most significant bit (MSB) of the differential value is '0' or '1', respectively. Ideally the counter should indicate '0' after testing is over because T_p and T_n should be equal. A margin of about ± 3 is given to obtain reliable results for the A/D converter test.

The block diagram of the bit fault detector is shown in Fig. 8. If the differential output value exceeds the normal value, the bit fault detector generates a fault signature. To

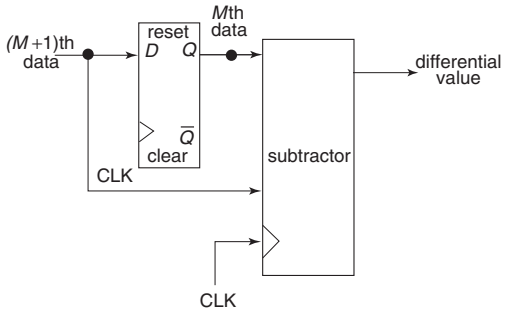

Fig. 7 *Differentiator*

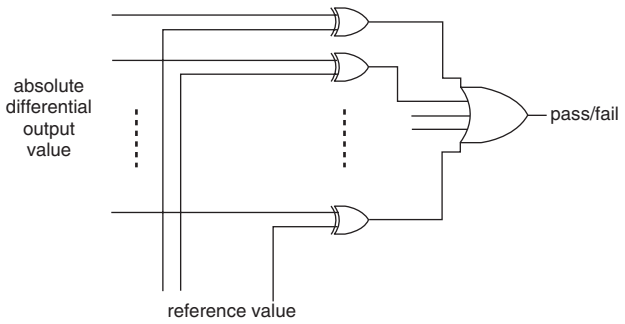

Fig. 8 *Bit fault detector*

obtain this result, the bit fault detector continuously compares the reference value with the differential value. It consists of several XOR gates and an OR gate.

Figure 9 shows the general implementation used in detecting SV and OSC faults. To compare three adjacent differential values, previous values are stored in D-type flip-flops. The detector verifies signals data1, data2 and data3: if they are all '0', the detector signals a SV fault; if adjacent values have a different sign bit, the detector generates an OSC fault signal.

4 Experimental results

In this Section, we present experimental results using the proposed BIST scheme and make a comparison with previous work.

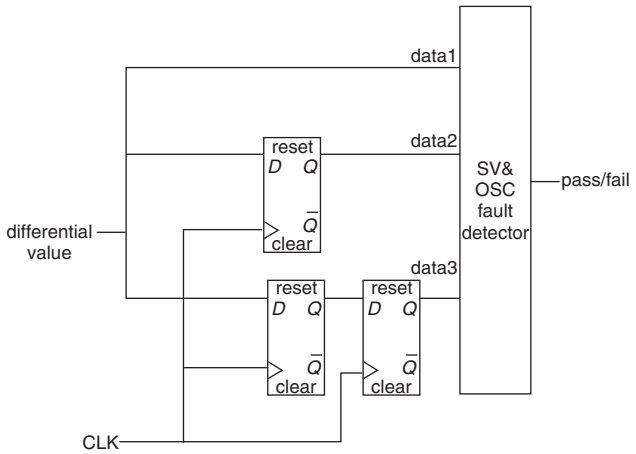

Fig. 9 *SV and OSC fault detector*

Experimental results show that at-speed testing is available. Moreover, experimental results for converters of different speeds show that the proposed BIST scheme is applicable to any A/D converter regardless of its speed. It takes only three periods of the input signal for the BIST to complete testing. Simulation results also show that the proposed ADC BIST circuit effectively detects not only catastrophic faults but also some parametric faults as well.

We use a Δ–Σ A/D converter and a pipeline A/D converter as benchmark circuits. These A/D converters are widely used in applications such as communication systems and audio systems. HSPICE was used to obtain the output of these A/D converters, and ModelSim was used to simulate the BIST and analyse the output of the A/D converters. To operate A/D converters as mixed-signal circuits, jitter can be introduced provided proper boundaries are set. We simulated the BIST several times to obtain threshold values to determine fault-free or faulty circuits and to fit boundaries for the jitter tolerance test. Following a substantial number of simulations, it was determined that an SV fault was detected when the differential output values of the A/D converter were three successive 0 s, and an OSC fault was detected when the difference between T_p and T_n was over ± 3. Bit faults were detected when the differential output values of the A/D converter were outside the designated range 5 to 7, used when testing the Δ–Σ A/D converter. When testing pipeline A/D converters, the bit

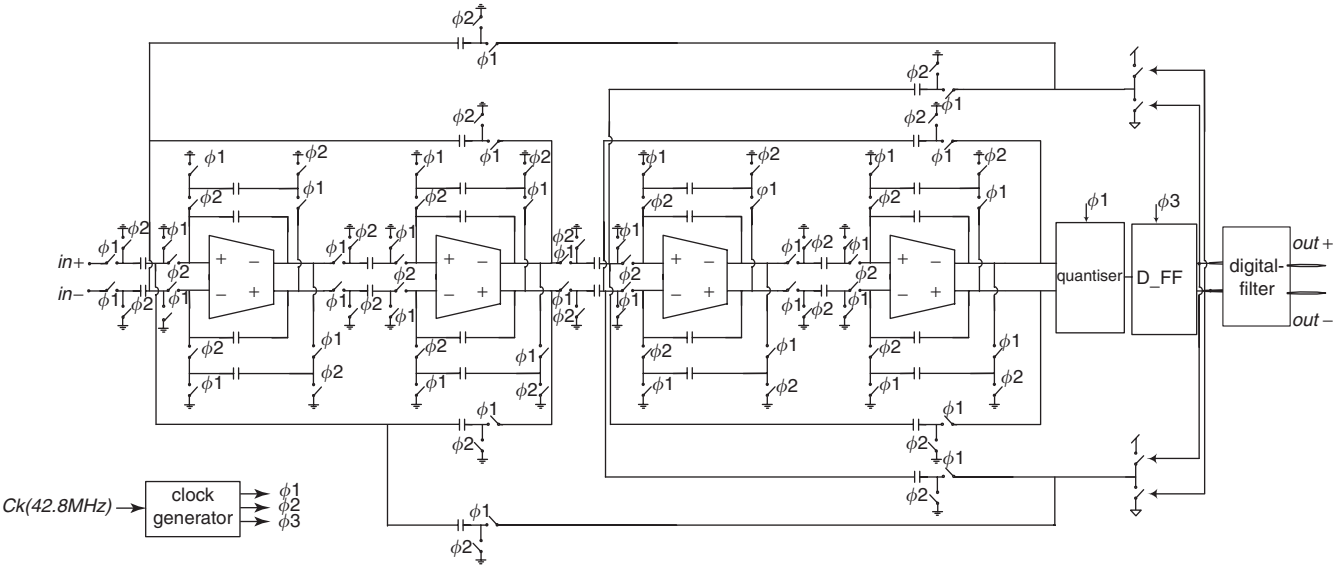

Fig. 10 *Δ − Σ A/D converter*

fault signal was generated when output values were outside the designated range 2 to 4.

4.1 Δ–Σ A/D converter

Oversampling Δ–Σ A/D converters have become very popular because they have the ability to solve problems inherent to other architectures, such as the need for high-accuracy analogue anti-aliasing filtering and high sensitivity to noisy environment. Because they offer high-precision conversion, conventional Δ–Σ A/D converters are widely used in low-bandwidth applications such as high fidelity audio processing. To calibrate the proposed BIST performance, we chose a 42.8 MHz 8-bit Δ–Σ A/D converter as the DUT. The input signal has to be sampled at a rate larger than the Nyquist frequency, so the desired test stimulus frequency is lower than 21.4 MHz. Therefore, we generated a 100 kHz triangular wave modulated with a frequency of 10.7 MHz using the A/D converter's internal clock. This provides the input signal to be applied to the Δ–Σ A/D converter to analyse the performance of the BIST.

A schematic of the fourth-order band-pass Δ–Σ A/D converter is shown in Fig. 10. The analogue test signal passes through the fourth-order building blocks, which consist of many OTAs and switched capacitors, and the result is quantised and stored. The edge-triggered D-type flip-flop storing the output of the quantiser is used to stabilise it as a 1-bit PCM code. The digital filter is employed to attenuate the quantisation noise within the band of interest so as to produce the desired SNR. It performs decimation of the output of the D-type flip-flop.

First, the BIST was applied to a fault-free Δ–Σ A/D converter to ensure correct discrimination. Fig. 11*a* shows the output signal of the A/D converter under fault-free conditions, and Fig. 11*b* shows the corresponding differential output of the A/D converter.

Since it is more reliable to test under steady-state conditions of the test stimulus generator, the BIST determines the output during the third period of the triangular wave, which is thought to be at steady state. Figure 12 shows that there are no faults registered, and therefore the DUT is fault-free.

Many simulations were performed with DUTs containing known faults. We provided test devices including catastrophic faults such as open or short circuit fault. Any fault in the device gives an A/D converter output signal that is distorted, like the signal depicted in Fig. 13.

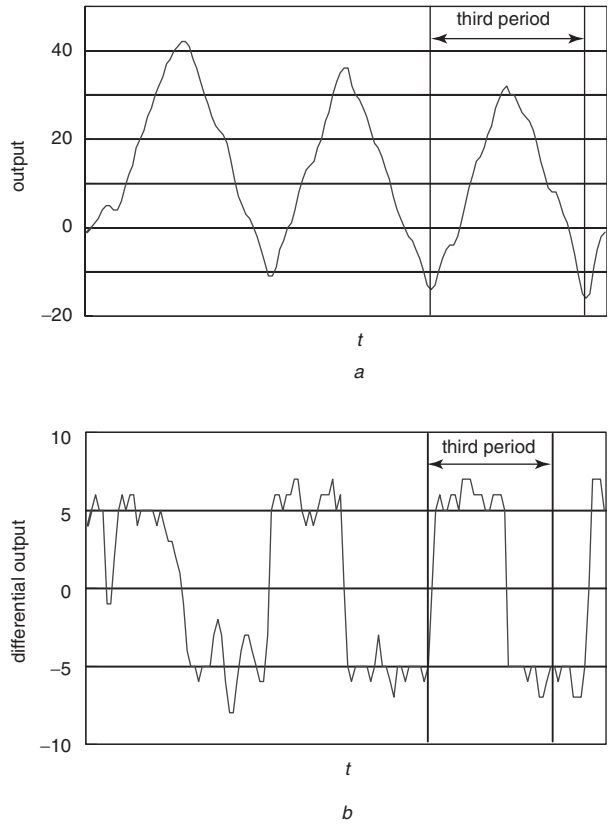

Fig. 11 *Fault-free operation*

When the BIST analyses circuits with faults, it generates a fault signature if it detects any of the three fault types. Figure 14 shows that there are faults in the DUT, detected through the BIST which is generating a 'check_out' bit as '1'.

There can be 930 faults in the DUT used in this simulation. The DUT is a fourth-order band-pass Δ–Σ A/D converter, so we can divide it into 4 blocks. A maximum number of 222 faults can exist in the first block, and maximum 228 faults in each of the other blocks. We have created a fault in the DUT several times and simulated the

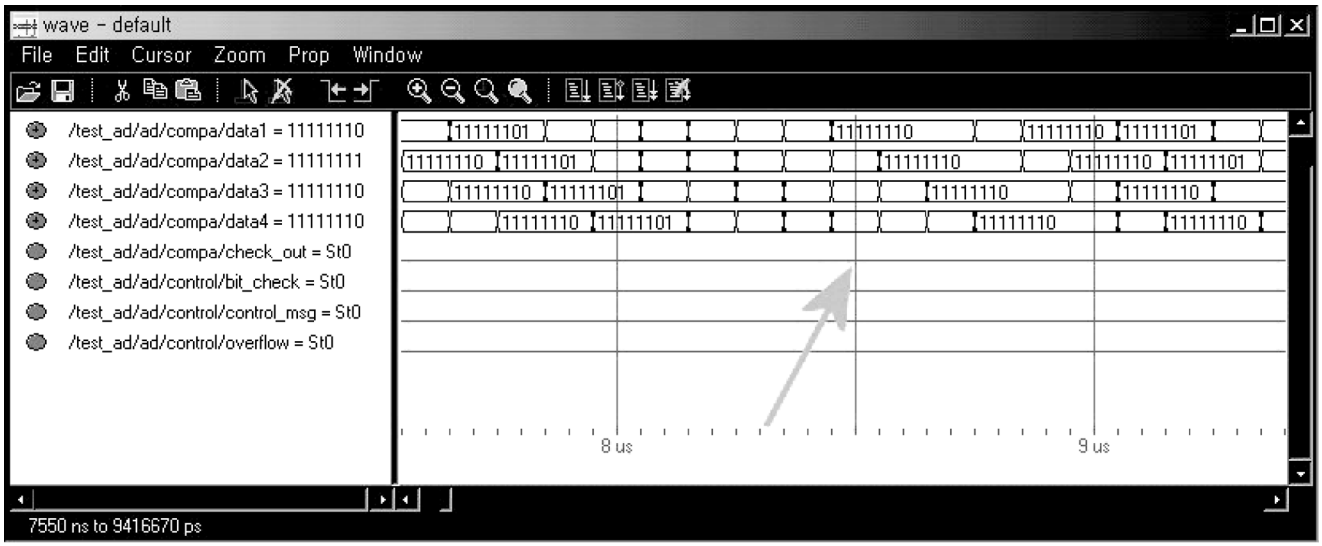

Fig. 12 *Simulation result in the fault-free case*

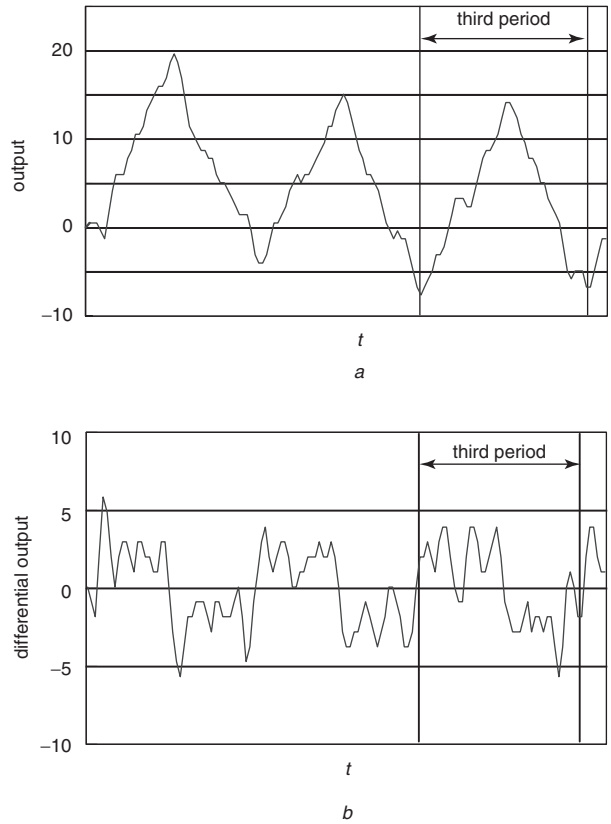

Fig. 13 *Faulty operation*

block. We can also expect the same results for the other blocks because the structure of each block is similar. However, to obtain reliable results, more simulations for second, third and fourth blocks are performed. As a result, we can obtain the same results as observed in the first block.

4.2 Pipeline A/D converter

In recent years, the pipeline A/D converter has emerged as an especially attractive A/D converter with medium-to-high resolution at medium-to-high conversion rates, so it has been used for large dynamic range data acquisition in communications applications. To measure the proposed BIST performance, we choose the 10 MHz 4-bit pipeline A/D converter as the DUT. The pipeline A/D converter device which is shown in Fig. 15 consists of four stages.

A maximum number of 516 faults can exist in the pipeline A/D converter. We randomly make 264 fault circuits and then simulated the BIST. We accomplish 132 fault simulations for the first stage and 44 fault simulations each for the others stages. Relatively a few simulations are done but the results are reliable because we randomly insert a fault in the DUT. The results of the BIST performance show that the proposed BIST has 100% fault coverage. Simulation results are shown in Table 2.

4.3 Comparison with previous work

A comparison of our BIST scheme with previous work is shown in Table 3.

The test method in [3] uses a narrowband filter for on-chip time-recursive implementation of an arbitrary

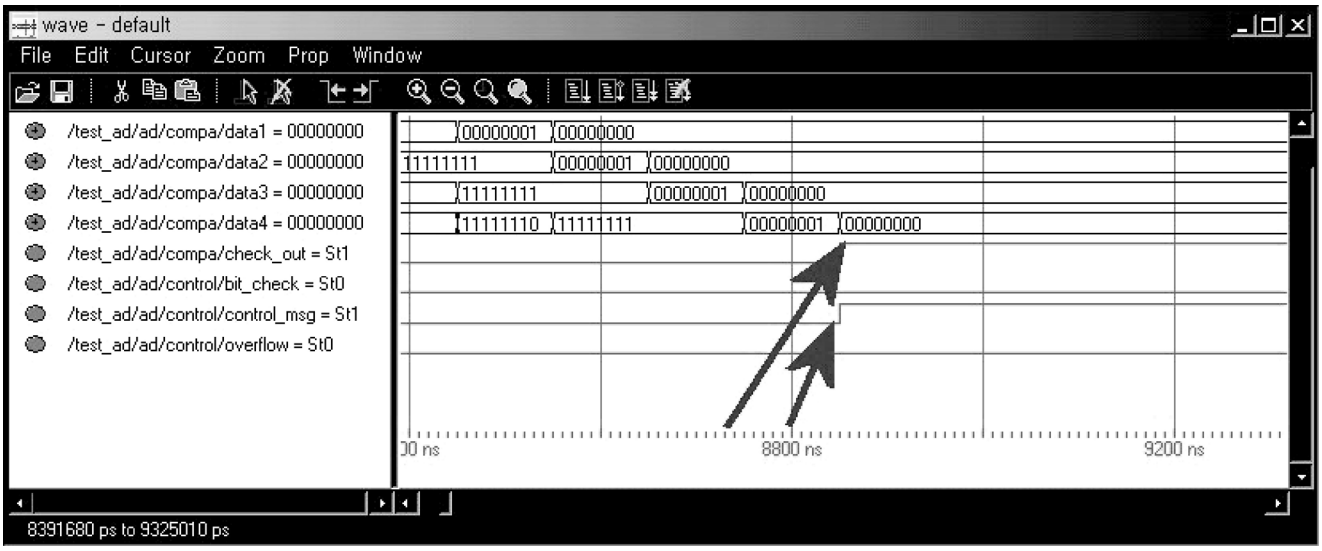

Fig. 14 *Simulation for faulty case*

performance of our BIST. The results are shown in Table 1. Through the simulation of the first block in all cases, we can conclude that the BIST has 100% fault coverage for the first

transform (such as a FFT) and a multitone signal generator for a test stimulus generation. There is indeed a cost in terms of extra circuitry and computational resources

Table 1: Test results for $\Delta - \Sigma$ A/D converter

	Test block1	Test block2	Test block3	Test block4	Nodes between test blocks
No. of total faults	222	228	228	228	24
No. of fault simulations	222	228	228	186	24
No. of detected faults	222	228	228	186	24
Fault coverage	100%	100%	100%	100%	100%

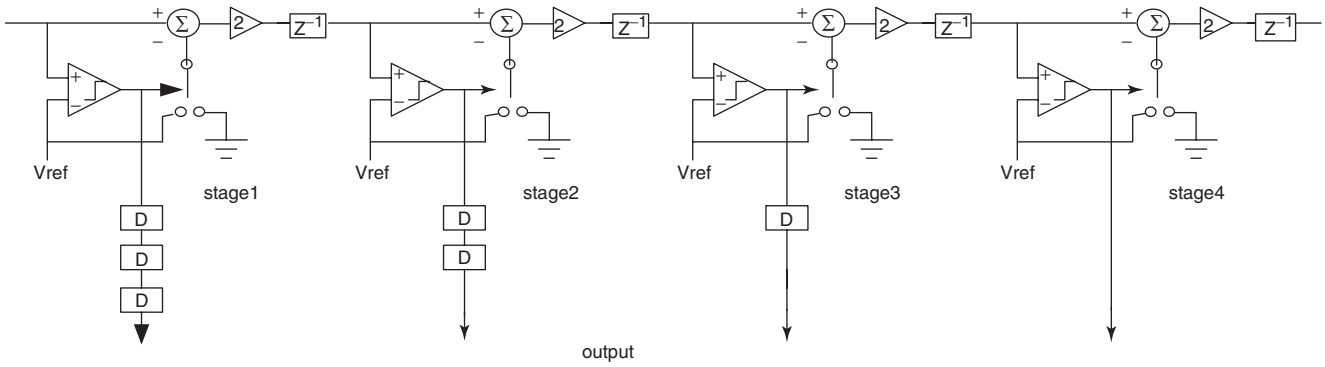

Fig. 15 *Pipeline A/D converter*

Table 2: Test results for pipeline A/D converter

	Stage1	Stage2	Stage3	Stage4
No. of total faults	132	130	128	126
No. of fault simulations	132	44	44	44
No. of detected faults	132	44	44	44
Fault coverage	100%	100%	100%	100%

for A/D converters which are typical analogue and mixed-signal circuits. We have defined three fault models of SV, OSC and bit faults to classify A/D converters as fault-free or faulty circuits and then implement the BIST to identify the three defined faults. The proposed BIST generates a triangular wave as the test stimulus and inserts it into the A/D converter and generates a pass/fail signal after analysing the output values of the A/D converter. To determine threshold values, an adequate number of simulations have been done to determine whether the A/D converter is faultless even though it is a faulty device. The experimental results guarantee that the defined fault models and the threshold values are pertinent. The advantages of the proposed scheme are not only low hardware overhead when compared with the histogram test technique which requires memory elements, but also there is no need for requirements like DSP resource and several successive periods of input signal. The new efficient BIST scheme reduces testing time and provides fault coverage results as high as 100%.

Table 3: Comparison with previous work

	FR, HD, and IMD test for BIST of a $\Delta - \Sigma$ ADC [3]	Towards ADC BIST scheme using the histogram test technique [5]	A self calibrated ADC BIST methodology [8]	Proposed BIST scheme
Test time	long	medium	medium	medium
Area overhead	medium	medium	very low	low
Requirements	DSP process D/A converter	none	none	none
Fault coverage	high	high	low	very high

required to implement the method. It has need of some requirements such as DSP resource and D/A converter, and it takes a long time to test because of waiting time for the filter to reach steady state and computing time for transforms. One of the most popular techniques used for external testing of A/D converters is the histogram test technique [5]. It is moderate in that the hardware overhead of the technique is 5∼10% compared to A/D converter's area, but hardware overhead and test time will be largely increasing when the higher fault coverage is needed. A self-calibrated BIST methodology presented in [8] requires only four resistors, a capacitor, a 4–1 multiplexer, and a control unit. The method minimises the hardware overhead utilising the on-chip processor in a SOC circuit, but fault coverage is low. The BIST scheme proposed in this paper achieves high fault coverage by suggesting the proper fault models and low hardware overhead by implementing BIST with only a triangular waveform generator, a BIST controller, a differentiator, and fault detectors.

5 Conclusions

In this paper, the efficient BIST scheme with high fault coverage and low hardware overhead has been proposed

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