J Electron Test (2008) 24:591–595
DOI 10.1007/s10836-008-5077-z

An Effective Power Reduction Methodology for Deterministic BIST Using Auxiliary LFSR

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Received: 29 May 2007 / Accepted: 30 May 2008 / Published online: 1 October 2008

Abstract Power consumption for test vectors is a major problem in SOC testing using BIST. A new low power testing methodology to reduce the peak power and average power associated with scan-based designs in the deterministic BIST is proposed. This new method utilizes an auxiliary LFSR to reduce the amount of the switching activity in the deterministic BIST. Excessive transition detector (ETD) monitors the number of transitions in the test pattern generated by LFSR and the low transition pattern is generated for excessive transition region using an auxiliary LFSR. Experimental results for the larger ISCAS 89 benchmarks show that reduced peak power and average power can indeed be achieved with little hardware overhead compared to previous schemes.

Keywords Linear feedback shift register · Built-in self-test · Reseeding · Power consumption

Responsible Editor: K. K. Saluja

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1 Introduction

Traditional test methods using the automatic test equipment (ATE) have become unsuitable for testing of these large SoCs. This is because the more IP cores are used in one SoC, the larger test data volumes are required. In order to apply this large volume of test patterns to the SoC, the ATE requires large memory and this increases the test cost of the SoC. Built-in self-test (BIST) is widely known as a good solution for testing the individual intellectual property (IP) cores in the modern system-on-a-chip (SOC). In BIST, there are two major problems, power consumption and testability. The linear feedback shift register (LFSR) reseeding methodology for high fault coverage in BIST was proposed in [3]. In this method, BIST loads a seed into an LFSR and the LFSR generates a deterministic test pattern and fills a scan chain set with the pattern. A seed can be computed for each test cube by solving a system of linear equations based on the feedback polynomial of the LFSR. However, it causes excessive power dissipation. In the LFSR reseeding scheme, the don't care bits in the test cubes are filled with pseudo-random bits generated by the LFSR and unnecessary switching activity is produced.

Several techniques for reducing switching activity in deterministic pattern generation have been developed [4–6]. A low power scheme using dual LFSR reseeding was proposed in [6]. In [4], a low power scheme uses hold cubes. In this scheme, each test cube is divided into several blocks and each block has a hold flag. In [5], a low power scheme based on scan slice overlapping has been introduced. But these schemes do not consider peak power reduction. Peak power consumption is critical issue in SOC test procedure. Excessive critical power requires more

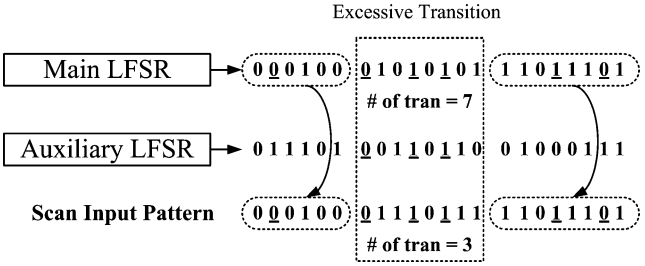

Fig. 1 Example of the low power pattern generation

expensive packaging and can permanently damage the circuits.

In this paper, a new low power testing methodology to reduce the peak power and average power associated with scan-based designs in the deterministic test pattern generated by LFSR in BIST is proposed. This new method utilizes an auxiliary LFSR to reduce the amount of the switching activity in the deterministic BIST. Excessive transition detector (ETD) monitors the number of transitions in the test pattern generated by LFSR. If ETD detects sections with excessive transitions in the test pattern, a low transition test pattern is shifted into the scan chain, instead of the original test pattern. The low transition pattern is combined two patterns generated by the original LFSR and the auxiliary LFSR.

2 Power Reduction Methodology

In the LFSR reseeding methodology, the don't care bits are filled with a pseudo-random pattern generated by the LFSR. These pseudo-random bits cause unnecessary transitions in the scan chain and increase peak power and average power. In the previous works for the deterministic low power BIST, the don't care bits are filled with specific values, instead of pseudo random value. Since these schemes focus on filling the don't care bits as many as possible and do not consider that corresponding don't care bits introduce high transitions in the scan chain, unnecessary filling operations are introduced for the don't care bits in the low transition sections of the test patterns. Also, according to the shape of the test pattern generated by LFSR, the reduction ratio of the transitions is not regular and the don't care bits not causing high transition may be filled with specific values. In the previous works, average power during test cycles can be reduced but peak power may not be reduced efficiently.

In the proposed methodology, ETD monitors the number of transitions in the test pattern generated by LFSR. If ETD detects sections with excessive transitions in the test pattern, a low transition test pattern is shifted into the scan chain, instead of the original test pattern. The low transition pattern is combined two patterns generated by the original LFSR and the auxiliary LFSR. While the original LFSR covers whole specific bits in the test cubes, the auxiliary LFSR covers partial specified bits which exist in the excessive transition sections detected by ETD in the original test pattern. If two values from the main and auxiliary LFSR are different, corresponding bit is a don't care bit in the test cube definitely. These don't care bits can be filled with a previous scan input value and a transition by this don't care bit is eliminated. The scan input pattern generated by this approach has 50% lower transition than the original pattern in the excessive transition sections. Figure 1 shows an example of the procedure for generating a low power test pattern. In the example, the underlined bits are the specified bits from the test cube. The auxiliary LFSR generates the specified bits in the dotted box detected by ETD. The test pattern from the main LFSR has seven transitions in the dotted box, while the pattern generated by the proposed method contains three transitions.

Power estimation models have been presented in [1]. Consider a scan chain of length l and a scan vector $t_j=t^*_{j,1}$

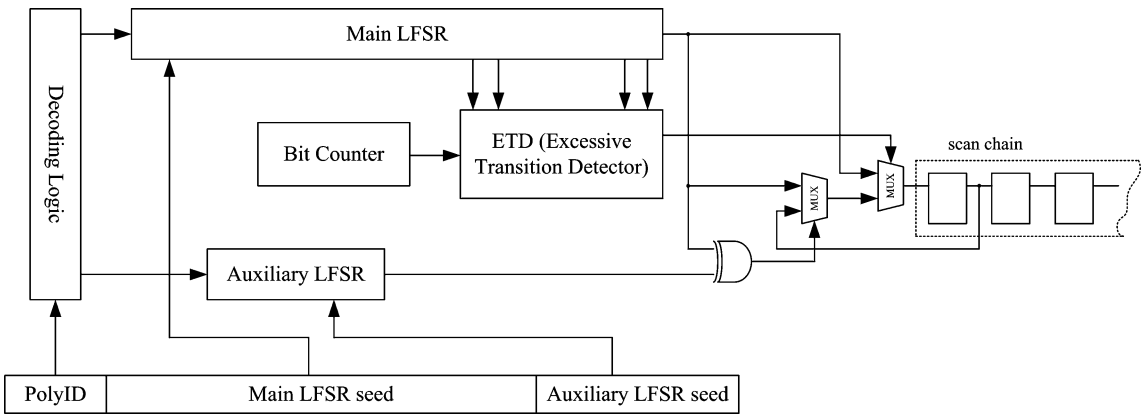

Fig. 2 Proposed hardware architecture

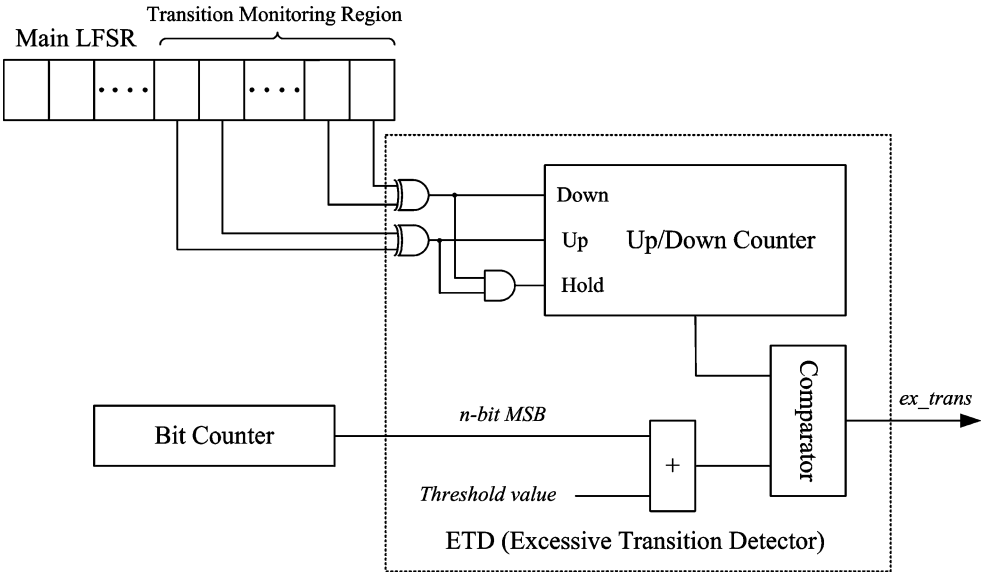

Fig. 3 Excessive transition detector (ETD) architecture

$t^*_{j,2}\ldots t^*_{j,l}$, with $t^*_{j,1}$ scanned in before $t^*_{j,2}$, and so on. For n vectors t_1, t_2, …, t_n, the average power and peak power are estimated as follows:

$$P_{\text{avg}} = \frac{\sum_{j=1}^{n}\sum_{i=1}^{l-1}(l-i)\cdot\left(t^*_{j,i}\oplus t^*_{j,i+1}\right)}{n}$$

$$P_{\text{peak}} = \max_{j\in\{1,2,\ldots,n\}}\left\{\sum_{i=1}^{l-1}(l-i)\cdot\left(t^*_{j,i}\oplus t^*_{j,i+1}\right)\right\}$$

Therefore, the transitions previously shifted into the scan chain dissipate more power than those late shifted. In order to reduce power dissipation efficiently, ETD changes the threshold value according to the position of scan vector. In the sections which cause much power dissipation, ETD lowers the threshold value and the auxiliary LFSR covers more specified bits in order to reduce more transitions than other sections. In the opposite case, ETD and the auxiliary LFSR operate conversely. Comparing the case using the constant threshold value, the number of specified bits which the auxiliary LFSR covers is similar, but much more transitions may be reduced.

3 BIST Architecture Using Auxiliary LFSR

Figure 2 shows the block diagram of the proposed BIST scheme. The proposed architecture consists of a main LFSR, an auxiliary LFSR, ETD, two MUX, and a XOR gate. According to the value of *ex_trans* (excessive transition) signal generated by ETD, a MUX adjacent to the scan chain selects test patterns from the main LFSR or the low transition patterns for the scan chain inputs. For the given test cube, the auxiliary LFSR covers the specified bits in the sections which *ex_trans* signal is asserted to logic 1. Therefore, both LFSRs generate the same outputs for the specified bits in those sections. The low transition patterns are made as follows. If the output values from two LFSRs are same value, the output of the main LFSR is shifted into the scan chain. Otherwise the previous scan input value is shifted into the scan chain to eliminate unnecessary transitions. Since the probability that two LFSRs generate the same outputs is 0.5, the number of the transitions can be reduced by 50% for the low transition patterns.

Table 1 Comparison of the proposed scheme with previous BIST schemes

Circuit	Dual-LFSR reseeding [6]		Hold flag reseeding [4]		Scan slice overlapping [5]		Proposed scheme		
	CR (%)	Tred (%)	CR (%)	Tred (%)	CR (%)	Tred (%)	CR (%)	ATred (%)	PTred (%)
S5378	79.44	25.04	NA	NA	70.38	NA	91.06	39.36	37.71
S9234	67.61	24.35	79	53	71.04	54.66	88.24	36.61	38.42
s13207	94.71	25.26	94	53	90.42	83.06	96.82	42.37	14.37
s15850	90.02	25.14	93	52	81.02	71.17	95.81	37.96	19.55
s38417	92.01	24.90	95	52	70.13	61.77	97.22	40.87	34.95
s38584	95.36	24.70	93	40	79.92	70.78	98.67	36.47	14.42

Table 2 Comparison of the proposed scheme with previous low power scheme

Circuit	Alternating run-length code [2]			Proposed scheme		
	CR (%)	ATred (%)	PTred (%)	CR (%)	ATred (%)	PTred (%)
S5378	NA	NA	NA	91.06	39.36	37.71
S9234	44.96	76.30	31.06	88.24	36.61	38.42
S13207	80.30	93.68	28.02	96.82	42.37	14.37
S15850	65.83	85.27	36.66	95.81	37.96	19.55
S38417	60.55	81.35	40.82	97.22	40.87	34.95
S38584	61.13	83.52	16.25	98.67	36.47	14.42

The structure of ETD is presented in Fig. 3. An up-down counter counts the number of transitions in LFSR. Two XOR gates detect input transition and output transition for the transition monitoring region, respectively. Since ETD detects instance transitions, the length of the transition monitoring region is very small. The AND gate holds the counter for case that the outputs of both XOR gates are logic 1s. A comparator checks the counter value exceeds the threshold transition value and generates *ex_trans* signal. An adder increases the threshold value gradually according to the position in the scan chain. The threshold value can be controlled in order to prevent structural damage, according to a threshold value of the given silicon or package.

4 Experimental Results

The experiments were performed on the largest ISCAS'89 benchmark circuits. For each circuit, automatic test pattern generation (ATPG) was performed to generate the deterministic test cubes for all faults targeting at 100% fault coverage. Each test cube was encoded into a main LFSR seed for the original test cube including whole specified bits. The specified bits in the excessive transition sections were selected and this new cube was encoded into an auxiliary LFSR seed.

Table 1 compares the results for the proposed scheme with previous low power BIST schemes. For the proposed scheme, threshold value has a range between 40% and 60% of the max transition in the transition monitoring region according to the position of the scan chain. For each scheme, CR represents the compression ratios, respectively. The compression ratio can be calculated by dividing the total amount of storage required to explicitly store the deterministic test patterns (the product of the length of the scan chain and the number of test cubes) by the amount of the encoded test data. Tred for previous schemes represents the reduction of the number of transitions. ATred and PTred for the proposed scheme represent the reduction of the average and peak transitions. It can be seen that the compression ratio of the proposed scheme for each circuit is higher than those of the previous schemes. In case of the previous schemes, the reduction of the peak power is not available. It can be seen that the proposed scheme requires much fewer transitions than [6] and the compression ratio of the proposed scheme for each benchmark circuits is higher than that of [6] in all cases. When compared to [3] and [4], the reduction of the average power is not as much as those found for other schemes, but those can be enhanced by changing the threshold value. Table 2 shows a comparison of the experimental results in previous low power testing scheme with the proposed scheme. While the average transition reduction is not reduced as much as for [2], similar peak transition reduction and much more compression ratio can be achieved.

The advantage of the proposed scheme compared with other schemes is that it can control the level of the power reduction using the threshold value of ETD. Therefore, the proposed scheme can control peak and average power in order not to exceed a threshold value and prevent structural damage to the silicon or to the package with high compression ratio. Figure 4 shows the relationship of the

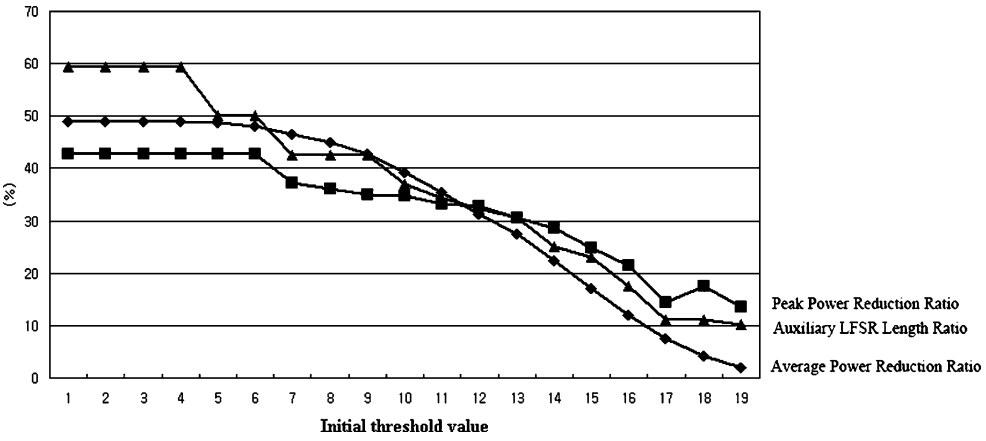

Fig. 4 Relationship of the power reduction and the auxiliary LFSR length with the threshold

power reduction ratio and the auxiliary LFSR length with the initial threshold value of ETD for s38417. The length of the transition monitoring region is 32 and the main LFSR length is 108. The threshold value must be decided with considering the power constraints of CUT.

5 Conclusion

Power consumption for test vectors is major problem in SoC testing using BIST. In this paper, a new low power testing methodology to reduce the peak power and average power in the deterministic BIST is proposed. This new method utilizes an auxiliary LFSR and ETD to reduce the amount of the switching activity in the deterministic BIST. Experimental results for the larger ISCAS 89 benchmarks show that reduced peak power and average power can indeed be achieved in all cases with high compression ratios. Since the proposed scheme can control the power reduction ratio using the threshold value of ETD, unnecessary and excessive effort to reduce transitions which do not exceed the threshold level and do not damage the devices can be eliminated.

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