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An Effective Built-In Self-Test for Chargepump PLL

Junseok HAN[†a)], **Dongsup SONG**[†], **Hagbae KIM**[†], **YoungYong KIM**[†], *and* **Sungho KANG**[†], *Nonmembers*

SUMMARY In order to provide an efficient test method for PLL which is a mixed-signal circuit widely used in most of SoCs, a novel BIST method is developed. The new BIST uses the change of phase differences generated by selectively alternating the feedback frequency. It provides an efficient structural test, reduces an area overhead and improves the test accessibility.
key words: *mixed-signal test, BIST, PLL*

1. Introduction

Analog and mixed-signal testing is becoming an important issue that affects both time-to-market and product cost of many modern electronic systems. An alternative approach to the success of products with satisfying these properties is built-in self-test (BIST) of circuits and systems. Related to a PLL BIST, most of previous works have carried out a functional test or a defect-oriented test on a open-loop state [1]–[3]. A defect-oriented test technique [1] controls the charge or discharge operation of the Chargepump and the Loop Filter. And this charge-based frequency measurement methodology is evaluated on the wafer test level with less sort-test time than a conventional test [2]. However this technique is not applied to a PFD(Phase-Frequency Detector) block. Simple digital tests for each of the various analog blocks are devised to use a standard digital tester [3]. However it has a loading problem for a sensitive analog node. In order to overcome these disadvantages, the new method puts emphasis on excluding a direct access to an analog node, reducing the number of pins for a test and minimizing the area overhead for a test.

2. Basic Theory

A structure of a CP-PLL(Chargepump PLL) is shown in Fig. 1 which is composed of a PFD, a Loop Filter and a VCO. Generally, stuck-at-1 and stuck-at-0 faults are easy to simulate using available analog circuit simulators. But open faults cannot be handled in a straightforward manner by breaking a signal path in the simulation input file. Inserting a high-value resistor to model this kind of faults likely leads to inaccurate results since the circuit behavior in the open fault cases might be unpredictable, whereas the resistor model produces deterministic results [4]. However the

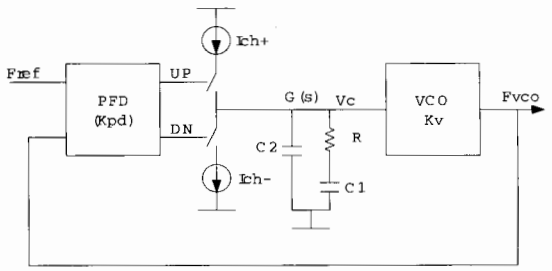

Fig. 1 A simple structure of chargepump PLL.

open faults of the blocks like PFD can be handled as transition faults or delay faults since they can affect the transition of the signal that passes by themselves [5]. Consequently, to detect these open faults, it is required to fully exercise the gates.

Thus, if some transitions on the negative feedback input frequency are changed, the faults in each block of a PLL can be exercised sufficiently. To do so, we use the frequency lock test on the closed loop state. If the feedback frequency is changed by the delay due to the open faults differently from the normal operation, the loop filter voltage increases or decreases and it affects the VCO output frequency.

Since the new technique gives some changes to the negative feedback input frequency, the faults which exist in each block of a PLL can be exercised. And the VCO output frequency can be counted by the frequency divider in the new BIST. So the VCO frequency can be extracted digitally [1], [3], [6]. Basically, the new technique in this paper is carried out without affecting normal PLL operations, and the new BIST technique is easily implemented with several counters and combinational logic gates. None the less, this method can test an entire PLL efficiently.

3. BIST Structure and Operation

The new BIST shown in Fig. 2 consists of a counter block for counting the reference frequency and the negative feedback frequency, a divide-by-4 block dividing a VCO output frequency by 4, a 2-by-1 MUX to select the VCO output frequency or the divided one, and a control-and-test_out block to control each counter and count the VCO frequency.

Figure 3 illustrates the operating procedure of the new BIST. Initially the FLT (Frequency Lock Test) is performed. When the feedback frequency is locked to the reference frequency, the lock signal gets a logic 1 state. During the lock

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[†]The authors are with the Department of Electrical and Electronic Engineering, Yonsei University, Seoul 120-749, Korea.
a) E-mail: seokju@samsung.com
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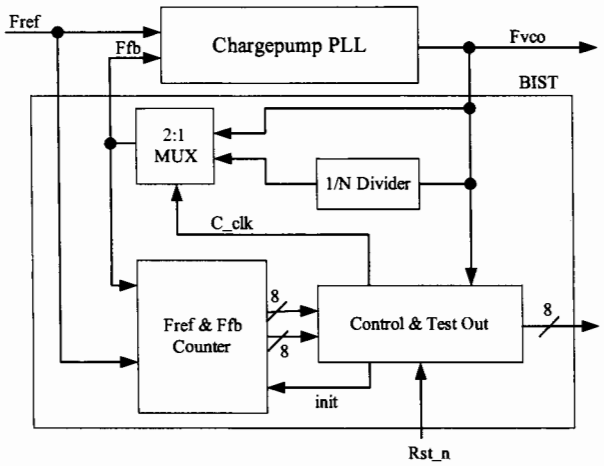

Fig. 2 The new BIST block diagram.

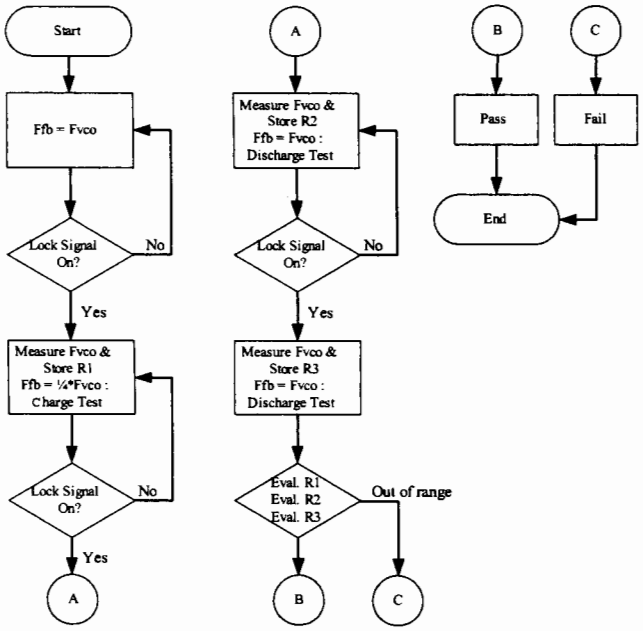

Fig. 3 The new BIST procedure.

signal maintains high, the feedback frequency is divided by 4 at the positive edge of the strobing signal generated from the BIST. So the VCO output frequency is increased and the feedback frequency is also increased. At the same time, the lock signal falls to logic 0 state. The reference frequency and the feedback frequency from the divide-by-4 block get into a locked state again. The lock signal goes to logic 1, too. And then, the MUX now selects the VCO output frequency to decrease the loop filter voltage, so the VCO frequency results in the same frequency as a reference frequency. This operation is repeated at the every positive edge of the strobing signal. The measurement of the VCO output frequency during the locked state is performed whenever the strobing clock is activated.

Figure 4 compares the loop filter voltage waveform with a Drain-Open (DO) fault in a PFD block and a faulty-free circuit. In Fig. 5, the lock signal waveform about these two are represented. These two figures explain the above operation procedures in two cases, which are a DO fault and a faulty-free. From Figs. 4 and 5, the VCO output frequency alternates between the reference frequency and the 4 times frequency. But since the feedback frequency gets locked to the reference frequency through a negative feedback, it appears that the effect of the DO fault is not observed. However, from Fig. 4, in a point of shifting one frequency to the other (A–E), the feedback frequency relatively increases or decreases to the reference frequency. At this time, each block of a PLL is fully exercised and the DO fault affects the transition. So the fault distorts or delays the loop filter voltage waveforms. Therefore the VCO output frequency is affected, and the fault is detected by the frequency. Furthermore, the test output is transformed into a digital value which can be evaluated with reliable digital circuitry.

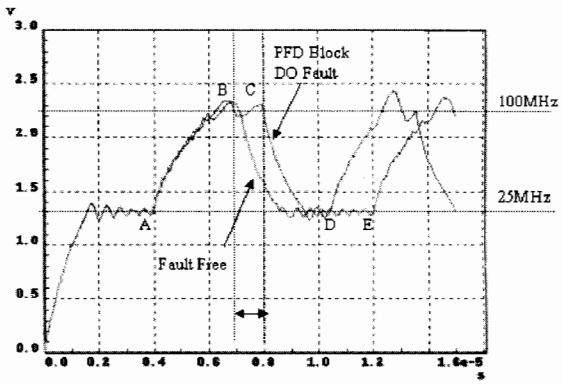

Fig. 4 DO fault—Fault free LF voltage waveform.

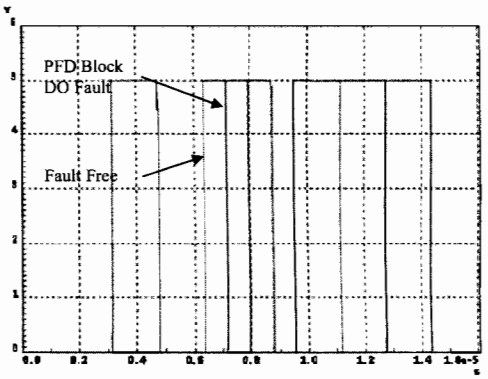

Fig. 5 DO fault—Fault free lock signal waveform.

4. Experimental Results

The target circuit of this paper is ITC97 PLL benchmark circuit, which is a classical type of CP-PLL like Fig. 1. For the experiment of this paper, Advance MS of Mentor Graphics Corp. is used [7]. The target circuit is simulated in a process of HP 1.2 μm.

The 6 fault models are applied for this experiment: Drain-Open (DO), Source-Open (SO), Gate-Open (GO),

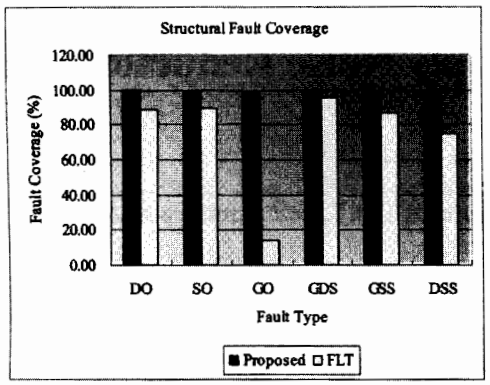

Fig. 6 Comparison FLT to the new method.

Gate-to-Source Short (GSS), Gate-to-Drain Short (GDS), Drain-to-Source Short (DSS). A transistor short is modeled by a small resistance (1 Ω) between the shorted nodes. A transistor open is modeled as a large resistance (10 MΩ) in series with the opened nodes. The target PLL uses 25 MHz as a typical frequency, the experiment is carried out with 7 bit counters from 20 MHz to 150 MHz frequency range so as to be 1.3 MHz (1%) for a strobing resolution.

The target PLL has totally 147 MOS transistors, and there are some short paths in terms of the characteristics in an analog circuit, such as a current mirror in a bias circuit. These short paths can be handled as untestable faults. Since the faults excluded by these short paths are totally 7 summing 5 GDSs and 2 DSSs, the total faults can be calculated as follows: $147 \times 6 - 7 = 875$. The FLT is carried out to prove the efficiency of the new technique. Figure 6 compares the fault coverage of both "FLT" and "Proposed" methods. As described above, the new method decides "Pass" or "Fail" from the evaluated binary number by 1% resolution. The average fault coverage of FLT method attains 77.69% at the most, but the proposed method yields 99.65% in the average fault coverage. And it appears that the new method has a higher fault coverage over the target faults from Fig. 6.

The comparison between the new BIST and previous works in terms of performance and characteristics is shown in Table 1. The new technique can test not only the faults of a PLL but also the frequency lock on-line in operation mode. This capability is useful for high reliability systems [6]. The new BIST can be easily implemented with only several counters and combinational logic gates. This technique can be applied to any chargepump type of PLLs due to the fact that it only connects with a VCO output and a feedback input node. The new BIST has about 600 gate counts, and this area overhead is relatively less than the previous method [8]. The new technique also has a simple test accessibility since it only uses a reference frequency and a test enable signal for a test. Therefore, the new technique which carries out a structural test is suitable for an efficient production test.

Table 1 Comparison with other recent PLL BIST techniques.

	[1]	[3]	[6]	[8]	Proposed
BIST Scheme	Defect Test	Defect Test	Functional Test	Functional Test	Defect Test
Loading Problem	Solved	Not	Solved	Solved	Solved
Loop Type	Broken	Broken	Not Broken	Broken	Not Broken
Area Overhead	Small	Small	High	Medium	Small
Test Access	Simple	Simple	Bad	Simple	Simple
Test time	Fast	Fast	Slow	Fast	Fast
Covered Block	Partial	Partial	N/A	N/A	All
Fault Coverage	Good	Bad	N/A	N/A	Best

5. Conclusion

This paper represents an efficient BIST method for the structural faults of an commonly used embedded CP-PLL in most SoCs. The new approach basically makes the test input stimulus applied to every block using the FLT. So it spends only a locking time to exercise all catastrophic faults in a PLL. The simulation results show higher fault coverage than previous test methods.

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