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LETTER

Noise-Tolerant DAC BIST Scheme Using Integral Calculus Approach

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SUMMARY This paper proposes a built-in self-test (BIST) scheme for noise-tolerant testing of a digital-to-analogue converter (DAC). The proposed BIST calculates the differences in output voltages between a DAC and test modules. These differences are used as the inputs of an integrator that determines integral nonlinearity (INL). The proposed method has an advantage of random noise cancelation and achieves a higher test accuracy than do the conventional BIST methods. The simulation results show high standard noise-immunity and fault coverage for the proposed method.

key words: *digital-to-analogue converter (DAC), built-in self-test (BIST), noise-immunity, static testing*

1. Introduction

As more mixed-signal circuits are implemented into a single chip, system reliability has become one of the most important factors in mixed-signal circuit design [1]. With regard to system reliability, ADCs and DACs, which convert processing data between analogue and digital, have been considered the bottlenecks in these systems. In particular, the DAC is a critical device in mixed-signal circuits, and its performance determines the accuracy and speed of an overall system.

For this reason, the testing of DACs is significant, although it has been regarded as a difficult task [2]. In many chips with high-speed and high-resolution DACs, the controllability and observability are generally low, so an expensive ATE is required to capture the low-level analogue data to test DACs. To overcome this problem, BIST approaches, cost-efficient and ideal solutions, have been studied.

However, conventional DAC BIST methods have some problems. In [3], a BIST scheme using a voltage controlled oscillator (VCO) to convert the DAC outputs into oscillation frequencies was proposed, and a DAC BIST scheme using a ramp signal as a pattern generator was proposed in [4]. These schemes are effective at reducing the number of reference voltages, but they require complex modules such as a VCO and a code/index memory. In this paper, a DAC BIST scheme with higher accuracy and no complex modules is proposed.

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2. Proposed BIST Scheme

The block diagram of the proposed BIST scheme is shown in Fig. 1. The system is composed of a pattern counter, an offset voltage generator, a linear ramp generator, amplifiers, and several basic modules. These test modules are assumed to have tolerance since they can be implemented without difficulty. The pattern counter provides an n-bit test pattern, and the differential nonlinearity (DNL) test module and INL test module generate the test data for DNL and INL testing. In addition, two capacitors store the data, and the switches control the open/closed states of the capacitors.

DNL testing: The proposed BIST performs the DNL and INL testing in parallel. When the DNL testing starts, the values of the offset voltage generator are selected, and Amp_1 calculates the differences between the DAC under test and the offset voltage generator. The DNL testing data from the DNL test module is stored in Cap_1 and Cap_2 in turn. Amp_3 calculates the voltage differences between the two capacitors, which replace the DNL. Finally, Amp_4 examines whether the values are within the desired accuracy by comparing the selected test reference voltage.

The offset voltage generator generates the voltages at four levels and it can be implemented using voltage division. Figure 2(a) shows the outputs of the offset voltage generator during the DNL testing. As the DNL testing proceeds, the output voltages of the DAC are generated as shown in Fig. 2(b). The offset voltage generator and Amp_1 alleviate the operation range of DNL test data to a quarter of original one, thus increasing the reliability of the BIST structure. The DNL data generated by *DNL test module* are shown in Fig. 2(c). Results of the DNL testing are acquired by the differences between two consecutive DNL data. The differ-

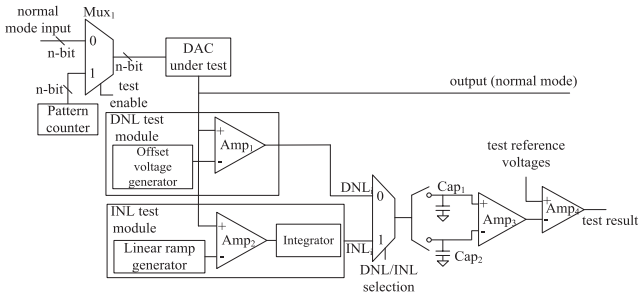

Fig. 1 Block diagram of the proposed DAC BIST.

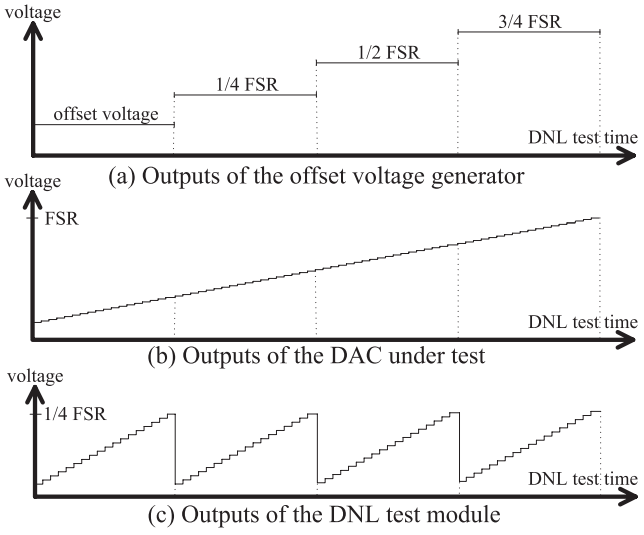

Fig. 2 Output signals for DNL test.

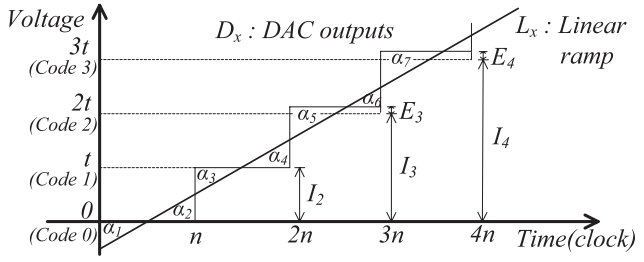

Fig. 3 Output signals of the DAC and the ramp signal.

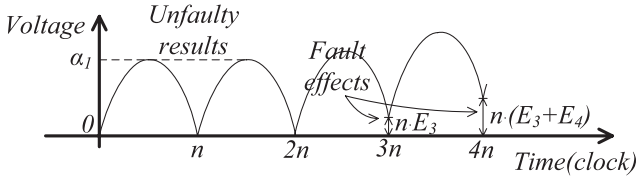

Fig. 4 Integral results for the difference between the DAC and the ramp.

ences are equal to 1 LSB, if the DAC under test works normally, except three drop-down points. In case of the drop-down points, the differences are equal to a quarter of FSR and the DNL test can be performed by adjusting the reference voltage.

INL testing: In INL testing mode, a linear ramp generator is activated instead of the offset voltage generator. The rest of the procedures are similar to those in DNL testing. Amp_2 calculates the differences between the DAC under test and ramp signals, and the results are integrated by the integrator. These INL testing data are stored in Cap_1 and Cap_2 in turn, and Amp_3 calculates the INL. Lastly, whether the DAC under test has a fault or not is determined by Amp_4. Amp_4 checks that the measured INL data are within the allowed range in the same way as the DNL testing.

Figure 3 and Fig. 4 show a mathematical principle of the INL testing method, where the tested period of DAC is set to n. Figure 3 shows the output signals of the DAC (D_x) and the linear ramp signal (L_x) during INL testing. In Fig. 3, differences between D_x and L_x are expressed as α_1, α_2, α_3, etc., and the integral results of the differences are plotted in Fig. 4. If the DAC has no fault, then all α_k have the same values. The integral values then converge to 0 for each of the rising and falling edges of the clock signal. However, if the DAC has faults, then each α_k has a different value, and the integral values converge to the specific non-zero value. The graph in Fig. 4 shows the value of $n \cdot E_3$ at the third clock cycle, which represents the accumulated INL error for three clock cycles. For the same reason, the error E_4 in Fig. 3 increases the accumulated INL error of the integral function in Fig. 4 by the amount $n \cdot E_4$. As a result, the function converges to $n \cdot (E_3 + E_4)$ at the fourth clock cycle. These procedures can be expressed using the following equation:

$$\int_0^{4n} (D_x - L_x)dx = n \cdot E_3 + \int_{3n}^{4n} \left(\left(3t + E_4\right) - \left(\frac{t}{n}x - \frac{t}{2}\right) \right) dx = n \cdot (E_3 + E_4) \quad (1)$$

To acquire the INL error information at each clock cycle (E_i), the proposed BIST calculates the difference between the two values ($n \cdot (E_i + E_{i-1})$, $n \cdot E_{i-1}$) and scales down the difference using Amp_3. It can be evaluated by the following equation:

$$E_i = \frac{1}{n} \left(\int_0^{ni} (D_x - L_x)dx - \int_0^{n(i-1)} (D_x - L_x)dx \right) \quad (2)$$

In the previous methods [3] and [4], the BIST schemes need to include the reference voltages for DAC outputs. For example, if the outputs of DAC are detected as I_3+E_3, I_4+E_4, etc., to acquire the INL errors E_3 and E_4, the information of the corresponding reference voltages I_3 and I_4 are also required. However, the proposed method does not require any information about the reference voltages in order to determine the INL errors, greatly reducing the hardware overhead and complexity.

3. Simulation Results

HSPICE simulations were performed to verify the effectiveness of the proposed method. All the mixed-signal circuits were designed using the 0.35 μm CMOS process with a 3.3 V power supply voltage. The ramp generator which could directly affect to the test accuracy was implemented by utilizing the schematics in [5].

The simulations were performed for the noise-immunity and test coverage of the proposed method. In the noise-immunity simulation, we applied the BIST method to 10-bit DAC and measured the maximum DNL and INL errors. In the simulation for the test coverage, we set an analogue fault model and inserted the faults into the 6-bit MSB part of the 10-bit DAC.

The analogue fault model used in this study included

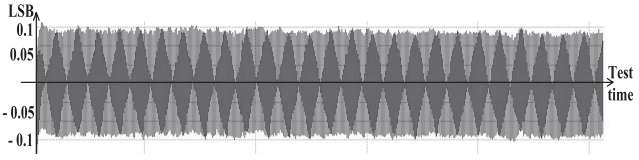

Fig. 5 INL testing results without noise.

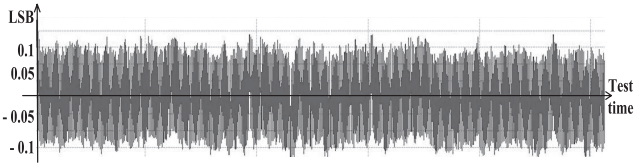

Fig. 6 INL testing results with Gaussian random noise.

Table 1 Results of the analogue fault simulation.

Fault	Fault coverage	Test coverage
DO, SO, DSB, GSB	100%	100%
GO	66.7%	91.7%
GDB	83.3%	100%
Total	**91.7%**	**98.6%**

the bridging and open faults, the most commonly observed physical failures in CMOS circuits [6]. The six faults applied in the experiments were gate-source bridging(GSB), gate-drain bridging(GDB), drain-source bridging(DSB), drain-open(DO), source-open(SO), and gate-open(GO). A transistor bridge is modelled as a connection between two nodes with a small resistance (1 Ω). A transistor open is modelled as a large resistance (10^8 Ω) in each node.

The waveform in Figs. 5 and 6 describe the INL simulation results of the proposed method. The INL testing results with noise affection are represented in Fig. 6, which shows the INL testing results influenced by the ± $2V_{LSB}$ Gaussian random noise. The Gaussian random noise data was generated through a C language. In the case of the result in Fig. 5, the maximum error was measured as 0.120 LSB. The proposed method was not affected by noise since the maximum value of the testing data in Fig. 6 is less than 0.147 LSB.

The noise tolerance of the proposed method exists because the method integrates the random noise as well as the output signals. This random noise can then be reduced by the integrator because its positive and negative values are cancelled. Therefore, random noise with a mean value of zero does not affect the test quality even if a high level of noise is included.

Table 1 shows the results of the simulation for the test coverage when the analogue fault model was applied. The fault coverage shown in Table 1 represents the ratio of the fault detection for the entire analogue faults. However, the fault coverage includes some inactive faults that do not affect the normal DAC operation, and these meaningless faults need to be ignored. To make up for the shortcoming, the test coverage is defined as the fault detection ratio for active faults which have harmful effects on outputs of DAC. As shown in Table 1, the proposed BIST provides an average of 98.6% test coverage, and the fault detection of the proposed method is demonstrated.

Table 2 Comparison with conventional method (N_t).

	S. Chang's scheme [3]	J. Huang's scheme [4]	Proposed BIST	
Maximum INL error (LSB)	**0.1** (8-bit DAC, $2V_{LSB}$ noise)	**0.046** (8-bit DAC, $1V_{LSB}$ noise)	**0.05** (8-bit DAC, $2V_{LSB}$ noise)	**0.147** (10-bit DAC, $2V_{LSB}$ noise)
N_t	0.05	0.046	0.025	0.01837

Table 3 Comparison with conventional method (coverage).

	J.Ramesh's scheme [7]	Proposed BIST
Test coverage	**95.22**	**98.6**

A comparison between the proposed scheme and previously published DAC BIST methods is summarized in Table 2. In order to carry out the comparison under the same conditions, we define a noise tolerance (N_t) applying the DAC resolution and noise amplitude. The N_t is expressed by the following equation:

$$N_t = \frac{INL\_error}{2^{(resolution-8)} \cdot (Noise/LSB)} \quad (3)$$

Table 2 shows that the reduction ratio of random noise in the proposed scheme was much higher than those in [3] and [4]. In the comparison of test coverage with analogue faults, the proposed method had greater test coverage than did the method in [7], as shown in Table 3. The proposed BIST also has the advantage of low hardware complexity compared with the method in previous works. The proposed BIST does not include complex modules like digital signal processors or memory, as were used in [3] and [4], and can be implemented with only transistors and passive components.

4. Conclusions

This paper presents a new BIST scheme for the efficient testing of a DAC. The proposed BIST uses the offset voltage generator for DNL testing and the integrator module for INL testing. These basic modules enable an area-efficient BIST with high noise-immunity, unlike conventional methods which require high hardware overhead. In addition, the proposed method achieves remarkable test coverage with regard to analogue faults.

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