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Pattern Mapping Method for Low Power BIST Based on Transition Freezing Method

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SUMMARY Proposed in this paper is a low power BIST architecture using the pattern mapping method based on the transition freezing method. The transition freezing method generates frozen patterns dynamically according to the transition tendency of an LFSR. This leads to an average power reduction of 60%. However, the patterns have limitations of 100% fault coverage due to random resistant faults. Therefore, in this paper, those faults are detected by mapping useless patterns among frozen patterns to the patterns generated by an ATPG. Throughout the scheme, 100% fault coverage is achieved. Moreover, we have reduced the amount of applied patterns, the test time, and the power dissipation.

key words: BIST, low power BIST, design for testability

1. Introduction

Power dissipation during testing is known to be significantly higher when compared to functional mode. Since excessive power dissipation during testing can damage good integrated circuits and contribute to yield loss and higher manufacturing costs, the power problem is an important concern in this field[1]. This paper is focused on the power problem related to a BIST (Built-in Self Test) scheme based on full-scan mode. Several techniques have been proposed to address this problem[2], [3]. These techniques have been aimed at solving the power problem by a modified pattern generator and scan cells, blocking logics, and sub-scan chains. However, these techniques have problems related to fault coverage degradation, hardware overhead, and complicated algorithms.

We have proposed a low power method based on the modified pattern generator, transition freezing method[4]. The purpose of [4] is to reduce scan switching activities by increasing the correlation between consecutive vectors. Since test patterns generated pseudo-randomly from an LFSR nearly satisfy a pseudo-random Gaussian distribution, we have adopted the concept of the freezing value to control the number of transitions. Throughout the scheme, we achieved a 60% average power reduction and a 30% peak power reduction in ISCAS’89 benchmark circuits. However, since the transition freezing method freezes over transitive transitions, a frequent occurrence of frozen regions might cause the non-detection of more random resistance faults when compared to the general pseudo random method. This leads to the increment of applied patterns as well as fault coverage degradation. Generally, when test patterns are applied to the CUT (circuit under test), it initially finds a great number of faults. However, as the number of applied patterns increases, the number of detected faults decreases for random resistance faults. This is the reason that the patterns generated pseudo-randomly are unable to reach their full fault coverage. Furthermore, since the frozen patterns froze over transitive transitions, it is harder to achieve full fault coverage. Therefore, as the number of applied frozen patterns increases, the test time and the power consumption can be slightly increased.

This paper presents a pattern mapping method for mapping the useless patterns that do not detect faults among frozen patterns to patterns detecting random resistance faults obtained by an ATPG. Though the basic concept of the pattern mapping method is similar to that of the bit-flipping method[5] and the pattern mapping[6], the proposed pattern mapping method does not treat of an LFSR-state of a deterministic pattern generator and its computational efficiency problem being addressed in [5] and [6], respectively. Moreover, the pattern mapping method is based on the low power pattern set generated by [4], the proposed method is specialized in the power problem related to [4]. And the proposed method is easy to get the flipped bit by only inverting the incompatible bit on the frozen patterns, the mapping effectiveness and simplicity is the best compared to another methods.

Through such a method, we can reuse the useless patterns and reduce the total number of applied patterns and the test time. This can lead to low power dissipation as well as 100% fault coverage. Moreover, since the configuration of the useless frozen patterns is almost the same as it was after adopting the mapping procedure, the low power effect of the transition freezing method was hardly influenced.

2. Pattern Mapping Method

The pattern mapping method is divided into two sub- sessions: the transition freezing session and the pattern mapping session. When the test mode begins, the frozen patterns generated by the transition freezing method are applied to a scan chain to detect easy faults of the CUT. Then, as the number of easy faults decreases for its detection, the fault coverage will be saturated. At that time, the pattern mapping session begins with the purpose of detecting random resistance faults. We can also divide the pattern mapping session into two operations: the mapping operation and the
matching operation. Let $U_{\text{set}}$ be the useless pattern set which does not detect any faults among frozen patterns and $T_{\text{set}}$ be the deterministic pattern set for detecting random resistant faults. The mapping operation is to map the element of $U_{\text{set}}$ which has the best mapping ability to $T_{\text{set}}$ by the calculation of the incompatibility between $U_{\text{set}}$ and $T_{\text{set}}$. The incompatibility is defined as the sum of the number of different bits between $U_{\text{set}}$ and $T_{\text{set}}$ as follows.

$$P_{U_{\text{set}}}(x_i) \neq T_{\text{set}}(y_i) \quad x_i \in \{\text{x}|p_0, \ldots, p_n\}, n = P_{\text{length}},$$
$$y_i \in \{\text{y}|t_0, \ldots, t_n\}, m = T_{\text{length}}, x, y \in \{0, 1\}$$

As shown in (1), the incompatibility is calculated by comparing the same bit position $i$ of each pattern, a $n$-length pattern $P_{U_{\text{set}}}$ of $U_{\text{set}}$, and a $n$-length pattern $T_{\text{set}}$ of $T_{\text{set}}$. Upon completion of the mapping operation, the matching operation changes the incompatible bit into the compatible one. Since the incompatible bit of $P_{U_{\text{set}}}$ is the exact reverse value of the compatible bit, we can obtain the matched bit only by inverting the incompatible bit $x_i$ as shown in (2). Furthermore, the transition freezing method has a feed-back loop for reapplying the last scan input. When the incompatible bit generates from an LFSR, the inverted bit for the matching will be applied by the feed-back loop.

$$P_{U_{\text{set}}}(x_i) \neq T_{\text{set}}(y_i) \Rightarrow P_{U_{\text{set}}}(x_i) = T_{\text{set}}(y_i)$$

Figures 1 and 2 show examples of the mapping operation and the matching operation, respectively. In Fig. 1, the incompatibility of $P_1$ and $T_1$ is larger than that of $P_1$ and $T_3$. Hence $T_3$ is selected for the mapping. Then, as shown in Fig. 2, the incompatible bit of $P_1$ is inverted to match it to the compatible bit with the same bit position as $T_5$. Consequently, the matched pattern $P_1'$ is determined and the feed-back loop produces the matched bit when the pattern counter and the shift counter indicates the mapping pattern ($P_1$) and the matching bit position (#39).

3. Flow of the Test Session Using the Pattern Mapping Method

The flow of the pattern mapping method is shown in Fig. 3. Initially, the transition freezing session is executed for generating low power frozen patterns from an LFSR. Throughout the fault simulation, detected faults and random resistance faults will be separated. Then the ATPG finds deterministic patterns ($T_{\text{set}}$) for random resistance faults. With the useless pattern set ($U_{\text{set}}$) among frozen patterns and $T_{\text{set}}$, the mapping operation and the matching operation are carried out and checked 100% fault coverage using the fault simulation. Finally, the control bit generator will be synthesized to produce control signals at the mapping pattern and the matching bit position according to information from the pattern counter and the shifter counter.

Before conducting the mapping operation, $T_{\text{set}}$ will be sorted according to the mapping ability so as to improve the probability of the mapping. Mapping $T_{\text{set}}$ (which has a lower mapping ability) in advance gives more opportunities for it to meet its optimal pair of $U_{\text{set}}$ since the amount of unmapped patterns is still abundant at the beginning of the mapping operation. The $T_{\text{set}}$ is sorted by the number of ‘01’ and ‘10’ of a pattern. Since frozen patterns consists of the same consecutive bit vectors due to the feed-back loop of the freezing block, 01 and 10 of $T_{\text{set}}$ are the reason for lowering the compatibility between $T_{\text{set}}$ and $U_{\text{set}}$. If the number of 01 and 10 is the same, the sorting is carried out on the basis of the minimum distance between ‘0 (1)’ and ‘1 (0)’ except 01 and 10. The short distance between them means that the distance of the same consecutive bits in a pattern is shorter than the long distance pairs. Therefore, we consider the short distance pairs as causing the mapping ability low. Figure 4 shows an example of the sorting result using a por-
tion of the patterns for s5378 of an ISCAS’89 benchmark circuit. After the sorting of $T_{set}$, the mapping operation begins from a pattern of the worst mapping ability for improving the probability of the mapping, as mentioned earlier.

4. Experimental Results

Figure 5 shows a block diagram of the pattern mapping method. The control bit generator consists of combinational elements to indicate the mapping pattern and the matching position using counting information from a pattern counter and a shifter counter. The MUX of the pattern mapping block determines whether the matched bit will produce or not. A ‘$T$-ff’ is attached for reducing the hardware overhead of the control bit generator. For example, in order to map a frozen pattern (000001111100001111010) of $U_{set}$ to a deterministic pattern (xxxxxxx0001xxxxxxx0xx) of $T_{set}$, the bold bit stream ‘1110’ should be inverted. The control bit generator may generate (000000010001000000000) by the $T$-ff instead of generating (000000011110000000000), which leads to a reduction in the consumption of combinational elements by the control bit generator.

The pattern mapping method is able to achieve earlier 100% fault coverage when compared to the transition freezing method since a far smaller number of patterns are applied as the mapping operation begins from the early pattern number of $U_{set}$. The reduced amount of applied patterns can lead to low power dissipation. Figure 6 details an example of the effect of the pattern mapping method using s5378.

Experiments were conducted based on patterns generated by ATALANTA. The power reduction ratio of the proposed approach was simulated in C++ and the hardware was implemented and synthesized by TSMC 0.25 $\mu$m. The power consumption is estimated by using weighted switching activity (WSA) in the same manner as [4]. Hardware overhead was measured by Synopsys Design Analyzer and the BIST architecture was implemented by Mentor Graphics LBIST Architect using a single full scan chain. As shown in the figure, the transition freezing session is achieved up to the #500 pattern of frozen patterns and the rest of the test mode is performed by the pattern mapping session. The total number of faults that should be covered by the pattern mapping session was 260 and all these faults are covered with 824 patterns by the pattern mapping method using $U_{set} = 1500$ and $T_{set} = 260$. Throughout the pattern mapping method, we have achieved 100% fault coverage using only 824 patterns saved 1176 patterns compared to the transition freezing method.

Table 1 shows experimental results using ISCAS’89 benchmark circuits. The columns labeled PI and SI denote the number of primary inputs and state inputs for each benchmark circuit, respectively. FC$_{pr}$ is the fault coverage based on pure pseudo-random patterns and FC$_{TPM}$ represents the fault coverage achieved from the transition freezing method. In order to compare fault coverage in a fair manner, we applied the same number of pseudo-random pat-
terns and frozen patterns for every benchmark circuit. The column labeled pattern mapping session denotes the start pattern number of the pattern mapping session. $U_{\text{set}}$ and $T_{\text{set}}$ represent the number of useless patterns and deterministic patterns, respectively, according to the start pattern number of the pattern mapping session. The final pattern number is the total number of patterns for the transition freezing session and the pattern mapping session achieving 100% fault coverage. $\text{FC}_{\text{PMM}}$ represents the fault coverage achieved from the pattern mapping method. Though fault coverage was saturated by random resistance faults in the transition freezing method, the pattern mapping method has achieved 100% fault coverage while using a far smaller number of patterns compared to [4]. As shown in the table, an average power reduction of 59.28% can be achieved compared to [4] with an average 16.48% hardware overhead for implementing the control bit generator. The pattern mapping method has achieved 100% fault coverage while using a far smaller number of patterns is used when compared to [4].

### References


