Summary
This paper proposes a new BIST (Built-In Self-Test) method for static testing of an ADC (Analog-to-Digital Converter) with transition detection method. The proposed BIST uses a triangle-wave as an input test stimulus and calculates the ADC’s static parameters. Simulation results show that the proposed BIST can test both rising and falling transitions with minimal hardware overhead.

Key words: ADC, BIST, static test, triangle-wave

1. Introduction
In static ADC testing, the histogram method is the representative test technique due to its simplicity. However, long test time and large area overhead are required for the histogram method to be applied in a BIST structure. Another approach to perform static testing is the transition detection method [1], [2]. In [1], a new BIST structure for ADC using the transition detection method is presented. While this method reduces the hardware overhead, in practice, the transient zone problem should be considered [2]. In [2], an advanced transition detector can remove unnecessary transitions in the transient zones.

These methods [1], [2] only use a rising ramp signal as a test stimulus; therefore falling transitions are not tested. During the repeated execution of static testing, some samples might be collected in the initialization phase of the sawtooth signal as shown in Fig. 1. That can reduce the accuracy of the test. Moreover, the rising/falling time may be different as the type of the ADC. Therefore, testing both transitions will provide accurate test results.

This paper proposes a BIST that uses a triangle-wave as a test input to test both transitions. The transient zone problem is also considered without much increase of the area overhead. Simulation results validate the well-testability and overhead efficiency of the proposed method.

2. Proposed Method
A block diagram of the proposed BIST is shown in Fig. 2. For accurate triangle-wave generation, the generator from [3] is used. An auto-calibrated triangle-wave generator produces test stimuli and the \( V_{\text{comp}} \) signal, which indicates the rising/falling phase of the \( V_{\text{out}} \). Based on the \( V_{\text{comp}} \) signal and the lower 2-bit \( (D_1, D_0) \) of the ADC’s output, the static parameters (offset, gain, INL and DNL) are calculated.

2.1 The Transition Detector
Like the transition detector in [2], the proposed BIST monitors \( (D_1, D_0) \) and generates the \( \text{Tran} \) signal. The difference between the two methods is that the proposed transition detector responds to both rising and falling transitions. The schematic of the proposed transition detector is shown in Fig. 3.

The transitions are detected using the \( V_{\text{comp}} \) signal. When the \( V_{\text{comp}} = 0 \) (falling transitions), \( D_1 \) and \( D_0 \) are...
inverted and therefore the two bits from the ADC seem to always be performing a rising transition. \( \{C_1, C_0\} \) means the next \( \{D_{1'}, D_0\} \) value and the \( \text{Trans} \) signal is activated when \( \{D_{1'}, D_0\} = \{C_1, C_0\} \). The flow chart in Fig. 3 shows the procedure of detecting both rising and falling transitions. The \( \text{Trans} \) signal is also activated when the \( V_{\text{comp}} \) is changed at the start/end of the rising/falling phase.

After the activation of the \( \text{Trans} \) signal, following a short delay, \( \tau_{\text{d}} \), the detection counter moves to the next value and waits for the next transition. The delay \( \tau_{\text{d}} \) determines the pulse width of the \( \text{Trans} \) signal. Using this \( \text{Trans} \) signal, the INL/DNL detector calculates the static parameters.

### 2.2 The INL Detector

The INL detector makes a comparison between the actual code transition levels (\( T_a[k] \)) and the ideal ones (\( T_i[k] \)). If the acceptable error range is \( \pm 1/2 \text{LSB} \), \( T_i[k] \) should be in the range of \( (k-1/2) \text{LSB} \leq T_a[k] \leq (k+1/2) \text{LSB} \).

As shown in Fig. 4, the proposed \((2+m)\)-bit counter provides the ideal code transition levels when \( m \) determines the resolution. For example, if \( m=1 \), 1 LSB is divided into two, meaning that a half LSB can be expressed.

The proposed INL detector does not include the stabilizer counter that was introduced in [2]. Instead, \( \{R_1, R_0\} \) starts 1 LSB earlier and compared with \( \{C_1, C_0\} \) from the transition detector, as shown in Fig. 5. As a result, the area overhead of the INL detector is reduced.

During the INL test, when a transition occurs, the \( \text{Trans} \) is first activated, and then the INL calculation is made. Finally, the detection counter counts up and waits for the next transition. The \( \text{Trans} \) is also activated when the rising/falling direction is changed and the INL test will also provide offset (\( T_o[0] \)) and gain (\( T_o[2^k - 1] \)). In this way, the proposed INL detector tests three static parameters – INL, offset and gain.

### 2.3 The DNL Detector

The DNL detector calculates the distance between consecutive transitions. For \( \pm 1/2 \text{LSB} \) of acceptable range, the equation to determine a DNL fault is \( 1/2 \text{LSB} \leq T_a[k] - T_a[k-1] \leq 3/2 \text{LSB} \).

In the proposed DNL detector, an \((1+m)\)-bit counter is used for the calculation as shown in Fig. 6. The upper 1-bit distinguishes the valid range and the lower \( m \)-bit divides 1 LSB. As shown in Fig. 7, the counter is reset whenever the \( \text{Trans} \) is activated and counts up until the next activation of the \( \text{Trans} \). The counter is set to have all ‘1’s at the end of the acceptable range. This setting simplifies the analyzer logic.

However, in any transition detection method, including [1] and [2], the \( \text{Trans} \) signal is activated asynchronously to system clock; therefore the distance of \( 1/2 \text{LSB} \) and \( 3/2 \text{LSB} \) cannot be implemented exactly. The maximum DNL measurement error in the transition detection method is \( 1/2^m \text{LSB} \). Therefore, for more accurate testing, the size of the counter, \( 1+m \), should be increased. \( m \) is finally determined after considering the INL/DNL test configurations.

### 3. Simulation Results

In order to validate the proposed BIST, its performance is evaluated. A 12-bit flash ADC is employed as a circuit-under-test and some parameter mismatches are inserted for fault checking. The ADC and triangle-wave generator are simulated using HSPICE while Verilog HDL is used for the other BIST logic. The triangle-wave generator is designed with the method of [3] and the max. INL and DNL is 0.21 and 0.17 LSB respectively.

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**Fig. 4** The proposed INL detector.

**Fig. 5** The timing diagram for the INL test.

**Fig. 6** The proposed DNL detector.

**Fig. 7** The timing diagram for the DNL test.
Simulation results of detecting faults in the fault-inserted ADC are shown in Fig. 8. The two outputs of the BIST report the existence of the faults, and monitoring with the ADC output informs us which transition is faulty. Furthermore, if the fault type is not needed to be known, an OR gate can be inserted to reduce the pin overhead.

Table 1 shows a comparison between previous and the proposed BIST. For the comparison of the hardware overhead, the gate count is calculated with 2-input NAND gates. In Table 1, the proposed DNL detector is a bit larger than the previous one when $m=2$. However, if $m$ becomes larger, the situation is reversed.

The proposed DNL detector simplifies the analyzer logic and has small hardware overhead. In other words, the proposed BIST requires small area for accurate (larger $m$) testing. As shown in the table, the proposed BIST is able to perform a static test of an ADC for both rising and falling transitions with reduced hardware overhead.

The proposed method tests with digital signal analysis by monitoring only the ADC output, regardless of the ADC type. The test input generator is adopted from the previous work and the performance is already proved. The three detectors in the proposed BIST are all digital circuits; therefore the possible error during the self-test is minimized. The proposed method will be developed into BISC (Built-in Self-Calibration) and implemented for verification as our future work.

4. Conclusions

An advanced ADC BIST, which is based on the transition detection method, is proposed. The proposed BIST uses a triangle-wave as a test input and performs the static test not only for rising transitions but also for falling ones. Furthermore, the use of a triangle-wave prevents inaccurate test results caused by the initialization phase of a saw-tooth wave. The proposed BIST tests offset, gain, INL and DNL while considering the transient zone problem. In addition, the optimized analyzer logic minimizes the amount of the additional on-chip circuitry.

References