Test Methodology for Low Power SRAM's

(Is Iddq test useful for Low Power SRAM's?)

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Abstract

The increase in integrity of the recent VLSI technology has enabled a trendy of small and portable applications. These portable applications, like notebook computers and cellular phones, need the high-performance and low-power consumption. In most of products the major power consuming elements are the memories. So the low power memory technology has been developed. But the test features have not been studied sufficiently. This paper provides the test methodology useful for the low power SRAM's. And simulation results for the Driving Source Line technology show how useful Iddq test is.

I. INTRODUCTION

Due to the recent advances in portable applications, the low power memory technologies have been developed so much [1-4]. The sensitivity of the sense amplifier was improved to operate the memory cell at low voltage level [1]. By amplifying the cell current using bipolar transistor, the memory cell can operate at low voltage level [2]. An extra circuit is added to control the cell reference level for high-performance and low power implementation [3]. And the memory architecture is divided to reduce the circuit capacitance [4]. So far diverse low power SRAM's architectures have been studied and developed. But the test features and fault models for low power SRAM's have not yet been studied sufficiently. In this paper the study started from the point of view that the behavior of the low power SRAM's aren't different from that of the traditional SRAM's. Therefore the functional voltage test using March algorithms is sufficient for their functional faults. But the fault models, which have the same behaviors as good circuits but increase the power consumption, cannot be perfectly tested by the traditional voltage test methodology. So we performed simulations on a low-power SRAM architecture and examined how the fault models for low power SRAM's behave. For Driving Source Line (DSL) technology [3], such fault models, which disturb the low power operation with the normal functional operations, exist. These fault models cannot be tested by the voltage test methodology because they don't change the voltage levels at primary I/O. But they increase the leakage current, which makes more power consumption than that of a good cell. In these fault models, I_{ddq} appears so that the Iddq test is required for the low power SRAM's.

This paper is organized as follows. Section 2 describes the DSL architecture is described. In Section 3, 4 the simulation results are discussed. Finally a conclusion is provided.

II. Driving Source Line architecture

The DSL cell architecture for high speed and low power memories is proposed [3]. A proposed DSL architecture is shown in Fig. 1. The DSL cell is similar to a conventional cell, but a difference between the DSL cell and conventional cell has a source line (SL) that is connected at a driver MOSFET. The SL is a negative in the read operation and a float state in the write operation.

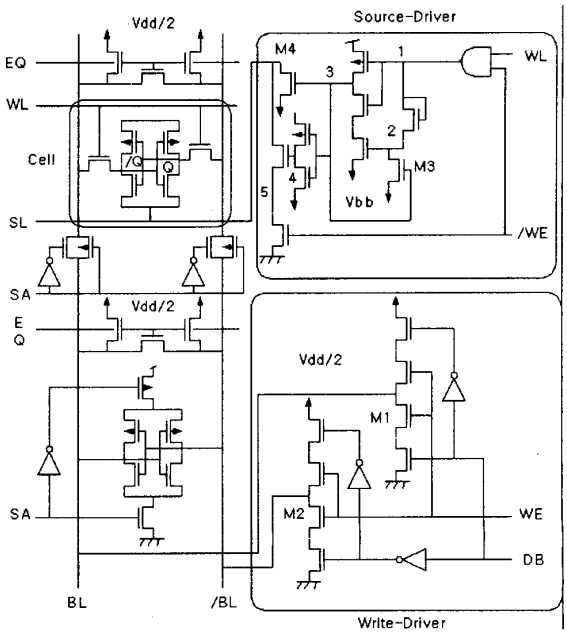

Fig. 1. DSL cell with an additional circuit

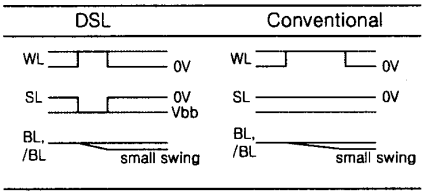

Fig. 2. Read operation comparison

The waveform of the DSL cell in a write operation and a conventional cell is shown in Fig. 2. If the WL (word line) is high, the SL is low. This makes a source substrate junction of the MOSFET applied forward bias and provides two effects.

First, a reduced threshold voltage increases a drain current of MOSFET due to a substrate bias effect. Second, it is a word-boosted effect that a negative SL drops the voltage of BL (bit line), besides it reduces the source voltage in the transfer MOSFET. Therefore, the DSL cell has highly a cell current and reduces the access time.

Compared with a conventional cell as a parameter of the Vth on the DSL cell, the relation between delay time and Vdd is as follows; the access time of the DSL cell is much faster

than Vdd, and a decline of delay time less immaterial rather than a conventional cell. Considering the power dissipation and delay time, the DSL cell is excellent at the power speed.

The waveform of a conventional cell and DSL cell in the write operation is shown in Fig. 3. While the WL is high, SL becomes a floating state. A conventional cell needs BL of the full swing to change the potential of BL, but in the proposed DSL cell, the voltage of BL is controlled by the small swing.

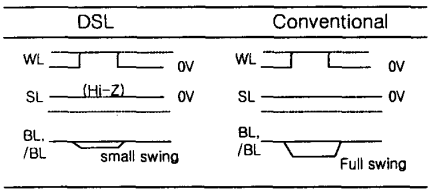

Fig. 3. Write operation comparison

III. Faults between the cell and the additional circuit

The simulation result of a normal circuit is shown in Fig. 4, where the simulation sequence is a write '1' operation, a read operation, and a write '0' operation by turns. Fig. 4 shows the write transition operation and a generated current pulse. The simulation is executed by the write operation with low voltage swing, and then it performs the low power operation.

It is possible to perform a read operation of the smaller cycle due to the decline of the SL in the read operation. Considering the fault of the low power memory, the faults in a cell is identical with the faults of a conventional memory, but the faults of the additional circuit may affect only power consumption. These faults of the additional circuit are classified into short faults, stuck-at faults of the internal additional circuit, and open faults. We will discuss the simulation result for the short between the cell and the additional circuit in this chapter, and the internal fault of the additional circuit in the next chapter.

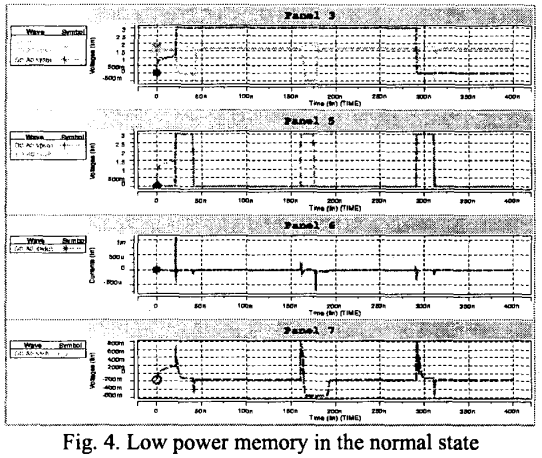

Fig. 4. Low power memory in the normal state

A. Short between the SL and BL

The simulation result for a short between the SL and BL is shown in Fig. 5. The short induces the unexpected state transition. Namely, the value between the BL and /BL causes state transition and generates the momentary current pulse. As Shown in Fig. 5, the opposite value of the actual write operation is stored in the memory cell, and in the next read operation the fault is detected by reading the opposite value of the write value. When in the next write '0' operation, the value of '0' is written correctly. Consequently, this fault is a stuck-at 0. Also, because this fault show in figure, generates I_{ddq}, it is possible to detect the fault with Iddq test. Similarly, a short between SL and /BL is detected as stuck-at 1.

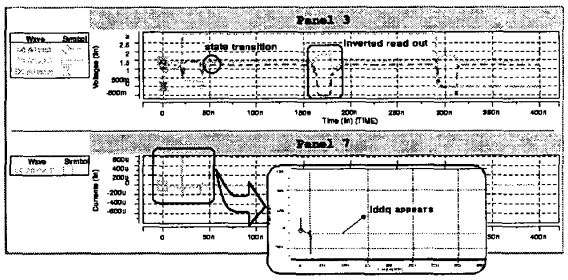

Fig. 5. Short between SL and BL

B. Short between the SL and Vdd

The simulation result for short between the SL and Vdd is shown in Fig. 6. In the read operation of the DSL architecture, the SL has to maintain high impedance. However, since the SL value is fixed to the stuck-at 1 by the short between the SL and Vdd, the actual SL value maintains not a negative value but the value of '1', which causes the uncommon operation that the voltage of M2 in the memory cell becomes high in the read operation. Therefore, the circuit becomes an unstable state that I_{ddq} is a nonzero. As a result the Iddq measurement in the read operation can test this fault.

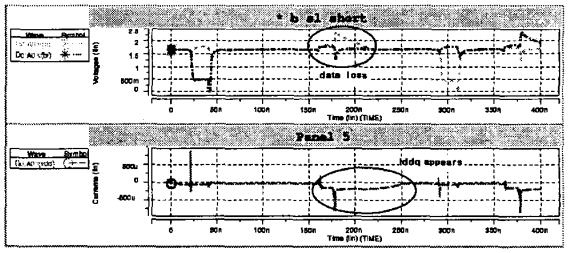

Fig. 6. Short between SL and Vdd

C. Short between the SL and WL

The simulation result for the short between the SL and WL is shown in Fig. 7. Considering the case of this fault, since the fault prevents the SL value from dropping in the write operation properly, the voltage variation differs little. Therefore, it is possible to detect the fault with the voltage test. Since the I_{ddq} isn't generated in this experiment, it is impossible to test the fault with the Iddq test.

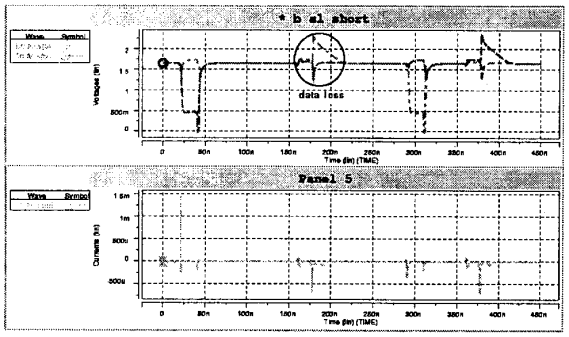

Fig. 7. Coupling fault between the SL and WL

D. Short between the SL and Q

The simulation result for the short between the SL and Q is shown in Fig. 8. This fault externally doesn't affect the functional operation of the memory, merely affects the low power operation. As shown in Panel 9 of Fig. 8, the transition write ('0' to '1'), is executed near 450ns and occurs at 500mV higher than the normal state. If the transition write ('0' to '1') occurs frequently, the power consumption of the memory is increased. But, this fault doesn't actually affect the functional operation of the memory. Hence, the short can't be tested by the voltage test. Since I_{ddq} is generated at about 53μA in the write transition ('0' to '1'), the Iddq test can only detect the fault. Similarly, the short between the SL and /Q increases the power consumption in the write transition ('1' to '0') and can be detected by Iddq test.

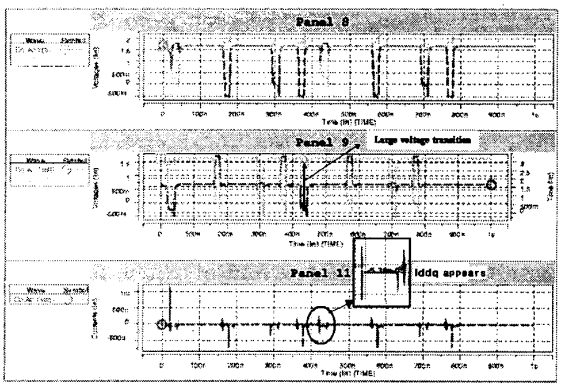

Fig. 8. Short between the SL and Q

IV. Faults in the additional circuit

The property of the stuck-at fault and the possibility of the voltage test and Iddq test is shown in Table 1. Since the I_{ddq} is the leakage current, it consumes the power. If the leakage current is generated, the power consumption increases as much though the circuit operates well functionally. Therefore, the I_{ddq} measurement can detect the fault which doesn't affects the function but disturb the low power operation.

Table 1. Property for stuck-at fault

Node	Fault	Description	Voltage	Iddq
M1	Stuck at 0	SL voltage level drop	X	O
	Stuck at 1	SL voltage level drop	X	X
M2	Stuck at 0	-	X	O
	Stuck at 1	SL voltage level drop	X	O
M3	Stuck at 0	SL voltage level drop	X	O
	Stuck at 1	SL voltage level drop	X	O
M4	Stuck at 0	SL voltage level drop	X	O
	Stuck at 1	-	X	O
M5	Stuck at 0	-	X	X
	Stuck at 1	SL voltage level rise	X	O
M6	Stuck at 0	SL voltage level drop	X	O
	Stuck at 1	SL voltage level drop	X	O

In the table, the fault property is classified largely into five types as follows. To begin with, the entire faults actually don't affect the functional operation. Accordingly the fault isn't detected with the voltage test.

Case 1. The SL value is not changed and the Iddq test cannot detect the fault (Stuck-at 0 at node 5).
Case 2. The SL value is not changed and the Iddq test can detect the fault (Stuck-at 0 at node 2 or stuck-at 1 at node 4)
Case 3. The SL value is increased and the Iddq test can detect the fault (Stuck-at 1 at node 5)
Case 4. The SL value is decreased and the Iddq test can detect the fault (The rest except stuck-at 1 at node 4)
Case 5. The SL value is decreased and I_{ddq} is generated in the read operation (Stuck-at 1 at node 4)

The stuck-at faults of the additional circuit basically generate I_{ddq} except the case 1. Since I_{ddq} is the leakage current, these faults disturb the low power operation though the circuit operates normally. The voltage test cannot test these faults because they cause the same functional operation like a good circuit.

The simulation result of the case 2 is shown in Fig. 10. The SL value is normal and generates the I_{ddq}. Although the operation of the case is normal, the power is consumed by the leakage current. Since the I_{ddq} (about 43.8μA) is generated continuously, the power consumption may be occurred continuously.

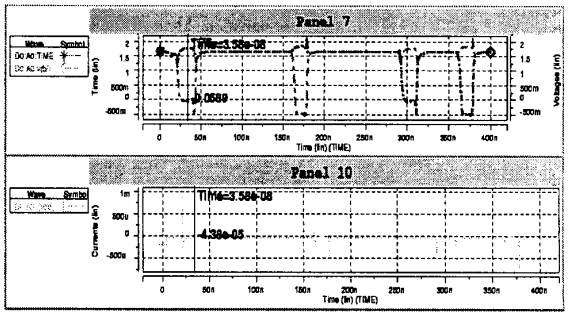

Fig. 10. Simulation result of the case 2

The simulation result of the case 3 is shown in Fig. 11. The voltage swing of the SL is increased and generates I_{ddq} (about 38μA). Since the SL of the additional circuit has a large voltage swing and the leakage current, the power consumption is increased rather than the normal state.

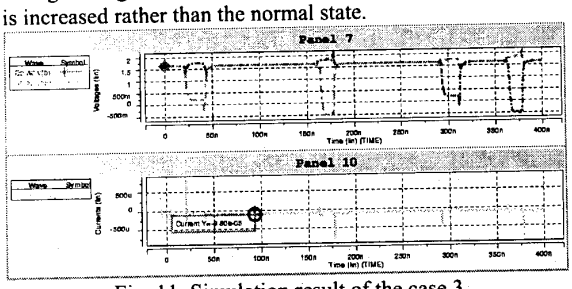

Fig. 11. Simulation result of the case 3

In the case 4, the SL voltage is decreased and generates I_{ddq}. The SL is the line that increases the difference in the voltage of the memory cell for the low power operation. This makes the read operation possible within the short range of the read operation. This means a continuous voltage supplies from the SL and can induce the power consumption. The simulation result of the case 4 is shown in Fig. 12. The SL value keeps the negative value not in the read section. It maintains the value about 0.1V in the actual case, but in the case 4 it maintains the value about 0.4V. This voltage supply increases the power consumption and generates I_{ddq} (37μA).

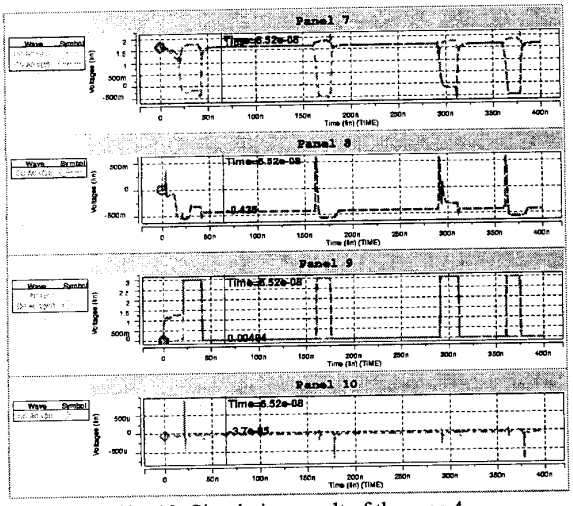

Fig. 12. Simulation result of the case 4

In the case 5, the SL value isn't changed; just I_{ddq} is generated in the read operation. Therefore, there isn't the difference in the power consumption during the write operation. Relatively large I_{ddq} is generated (0.2mA) in the read operation. Namely, it is possible to increase the power consumption in an application that has frequent read operations. Obviously, this fault can test with not voltage test but Iddq test because it is identical with the normal state functionally.

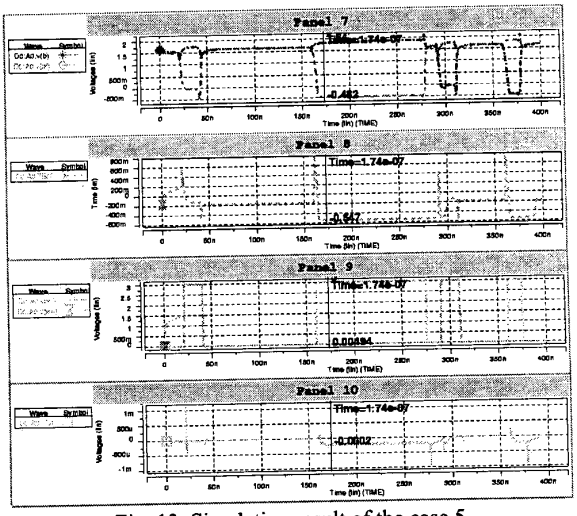

Fig. 13. Simulation result of the case 5

V. Conclusion

In this paper, the test methodology for low power SRAM's is discussed. In general, low power SRAM's are implemented by including extra circuits to reduce the operating voltage level or reducing the capacitance by dividing the memory circuit. If there exist fault models that do not affect the functional operation but the low power operation, they cannot be tested fully by the traditional voltage test. The simulation reveals that there exist fault models to disturb the low power operations without changing the normal behavior. Therefore in this paper proposes the Iddq test methodology for low power SRAM's. The results show the Iddq test is useful for testing low power SRAM's since the leakage current of the circuit can increase the total power consumption.

Acknowledgement

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