Delay Test for System on Chip

Sungho Kang/Yonsei University (Invited)

Delay Test for System on Chip

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Outline

- Delay Test Overview
- System-on-Chip and Its Test
- Delay Test for System-on-Chip
- Conclusion

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Delay Fault

- Failures that cause circuits to malfunction at desired clock rates or not meet timing specifications
- Modeled defects that cause signal propagation delays in a circuit to increase the modeled delays

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Delay Testing

- Checks if a circuit has delay faults or not
- Determines input patterns to be applied to detect and locate delay defects
- Requires at least two clock cycles
- Various types according to hardware models

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Transition Fault Model

- Not-rising fault and not-falling fault
- In CMOS transistor, stuck-open faults can be treated as faults that prevent the occurrence of certain transitions
  - So, important in CMOS-specific circuits
- It can be detected simply by combining single stuck-at tests over a sequence of two consecutive patterns

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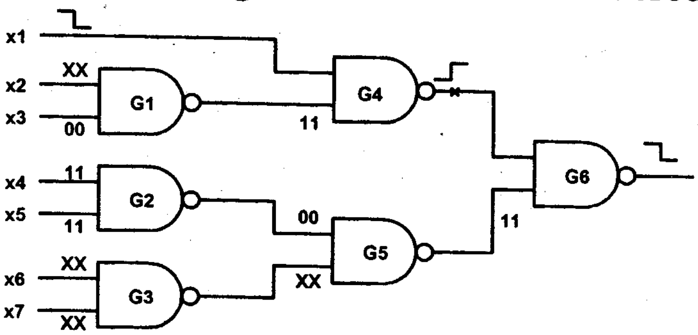
Gate Delay Fault(GDF) Model

- Localized defects only
- All possible single GDF can be considered



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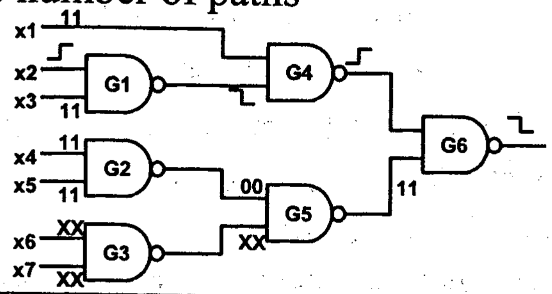
Path Delay Fault Model

- Can test both lumped & distributed defects
- Effective in statistical design philosophy
- Large number of paths



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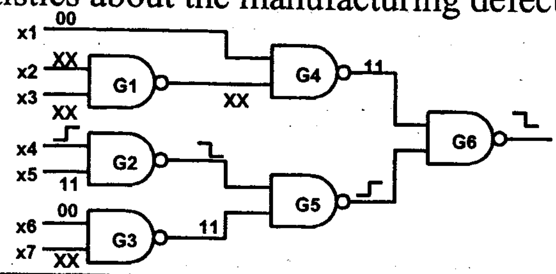
Segment Delay Fault Model

- Hybrid type of gate and path delay models
  - Slow-to-rise and slow-to-fall defects on segment, whose length L can be chosen from statistics about the manufacturing defects



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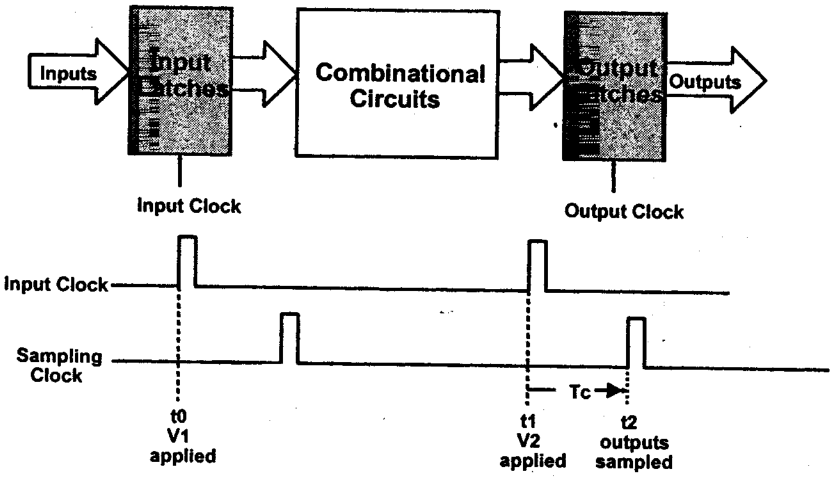
Hardware Model



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Combinational Circuits

Test Strategies

- Application of two patterns
  - Tests <V1, V2>, <V2, V3>, ...
  - Apply V1 and let the signal settle
  - Apply V2 and sample outputs after desired time
  - Let the circuit settle under V2
  - Apply V3 and sample outputs after desired time

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Sequential Circuits

Test Strategies

- Pure sequential circuits
  - Use fast and slow clocks
  - Too difficult
- Enhanced scan designs
  - Require additional chip area
- Standard scan designs
  - Difficult to handle sequential part of the circuit
  - Scan shifting problem

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Non-standard Scan Designs

Test Strategies

- Tests <V1, V2>, <V2, V3>, ...
  - Use a third latch to hold V(i) while V(i+1) is being shifted in
- Initializing and fault effect propagation may require slowing down the clock
- At speed testing may be feasible in initializable circuits

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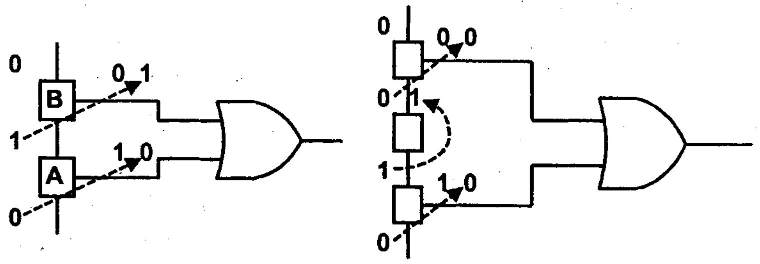
Standard Scan Designs

Test Strategies

- Scan shifting



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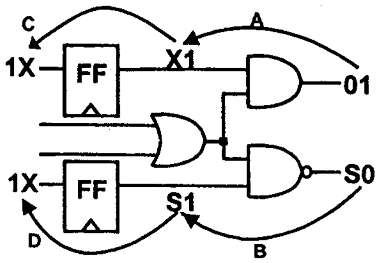
Standard Scan Designs

Test Strategies

- Functional Justification
  - The first vector can be scanned into flip-flops
  - The second vector is determined by function of circuits



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Gross Delay Faults

- Gate delay faults
  - Detectable along any path including the fault site
- Transition faults
  - Model gross delay defect
- Combinational/Scan
  - Single model is sufficient
- Non-scan sequential
  - Single model is sufficient if clock period can be controlled
  - Multiple fault models are needed if only the normal clock is used

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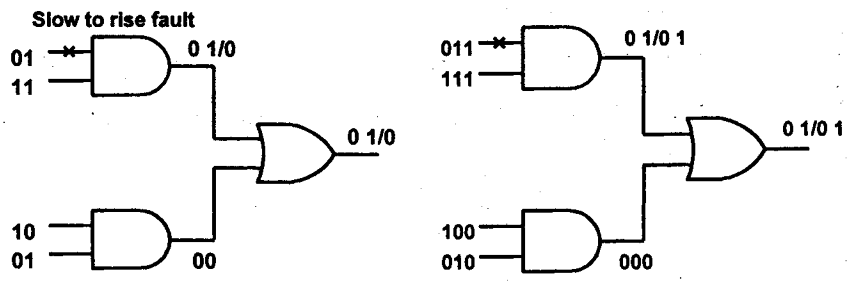
Transition Faults

Test Strategies



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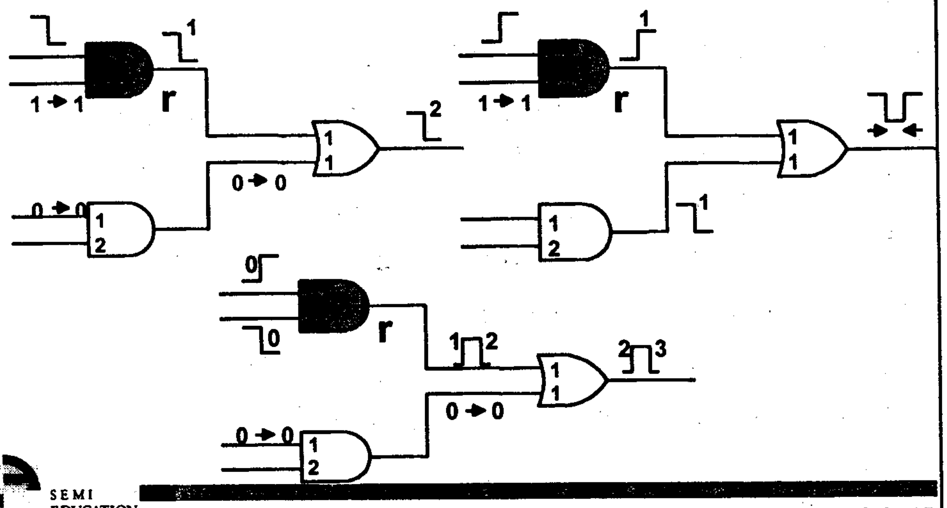
Gate Delay Faults

Test Strategies



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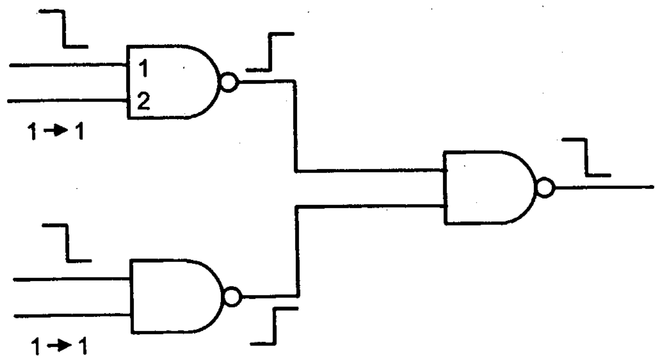
Path Delay Faults

Test Strategy

- Multiple path propagating



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Robust Test

Path Delay Test

- Hazard Free Robust Test [HFR]
  - Guarantees the signals on the path are free from dynamic hazards
  - Guarantees to detect the delay defects independent of the delays in other circuits
- Robust Test [ROB]
  - Guarantees to detect the delay defects independent of the delays in other circuits

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Robust Test

Path Delay Test

- Advantages of Robust Tests
  - Inaccuracies in circuit delay models tolerated
  - Tests valid even if the technology, clock rate or layout changes occur, as long as the logical topology is not changed
  - Used for binning

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Requirements for Robust Test

Path Delay Test

- Hazard Free Robust
  - Hazard free constant values for all off path inputs
- Robust
  - First vector : On-path elements must have initial values according to the specified transition types
  - Second vector : On-path elements must have final values due to the on-path fanin values

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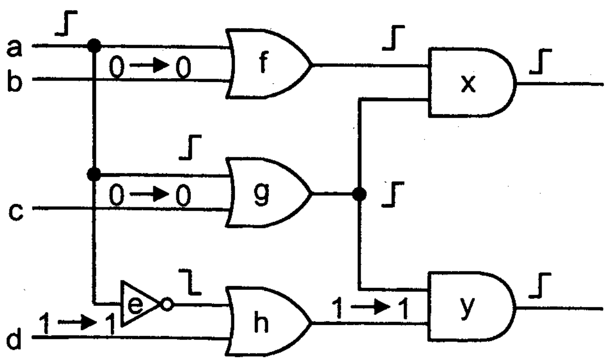
Robust Test

Path Delay Test

- Multiple path propagating hazard-free



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Transition Faults

ATPG(Automatic Test Pattern Generation)

- Combinational logic circuits or non-standard scan designs
  - 100% fault coverage can be obtained if 100% stuck-at fault coverage is achieved
- Standard scan designs
  - In general, <100% fault coverage is achievable

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Sequential Circuits

ATPG for Path Delay Faults

- Chakraborty, Agrawal, Bushnell
  - The only reported research
  - Too Low Fault Coverage
  - Too Long Test Time
  - Very Memory Insentive

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Standard Scan Design

ATPG for Path Delay Faults

- FASTPATH
  - Scan Based Microprocessor Design
  - Path Delay Models
  - Set of Longest Paths
  - Binning
  - Least Memory Intensive Approach
  - The most restrictive test is considered first

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28-Valued Logic

FASTPATH

- All Combinations of 0,1, X and Z
  - 00 01 0X 0Z 10 11 1X 1Z X0 X1 XX XZ Z0 Z1 ZX ZZ
- Logic Y : Constrained X + Z
- Stable Values
  - S0 S1 SZ
- Stable Impossible Values
  - 00T 0XT X0T XT0 11T 1XT X1T XT1 XTB

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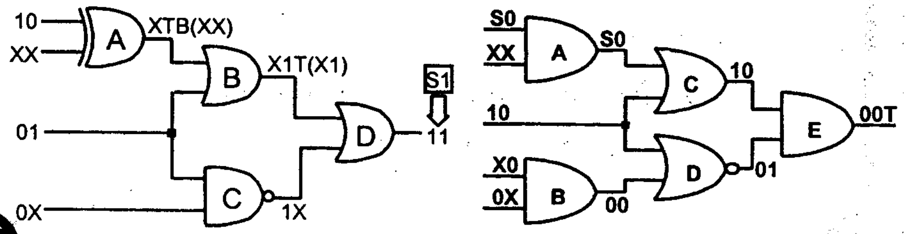
28-Valued Logic
FASTPATH

- Stable Impossible Values
  - T Indicates the signal would not be stable through both time frames
  - Can avoid unsuccessful searches



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Test Generation Algorithm
FASTPATH

- Least Memory Intensive Approach
- Reverse Time Processing
  - Begin with last time frame and proceed backward in time
  - state transition : transfer logic values between outputs and inputs of flip-flops
- Treat Flip-Flops as other elements
  - Set next state at time frame 1 using values of present state lines at time frame 2

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Delay Fault Simulation

- Ensures target faults are tested by the generated vectors
- Other sources of vectors
  - Functional vectors
  - Vectors that designers provide
- Useful for large sequential circuits

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Testability Measure

- The problem of simulating large number of path delay faults
- A solution that estimates the fault coverage without relying on path enumeration
- Extensions to increase accuracy
- Experimental results to demonstrate the effectiveness of the solution

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Testable Design

- Most of robust path delay fault testable circuits
  - Most methods developed are for combinational circuits
  - Most methods applicable to flattenable circuits only, as the starting point is two level circuits
  - Some results available for non-flattenable circuits, but methods that are generally applicable are yet to be devised

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SOC Design Paradigm

- Emergence of Very large transistor counts on a single chip
- Mixed technologies on the same chip
  - Logic, Analog, Memory, Processor
- Creation of Intellectual Property (IP)
- Reusable core-based design
  - Cores replacing standard parts, such as DSP, DRAM, MCU, Flash, and FPGA

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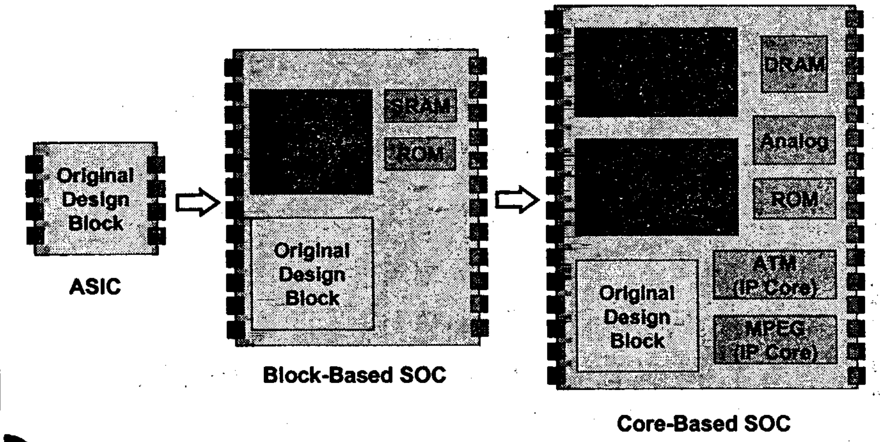
SOC Evolution



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IP Core types

SOC Test

- Hard Core(Technology dependent layout)
  - Predictable area and performance
  - Lack flexibility
- Soft Core(RTL)
  - leave much of the implementation to the designer
  - Flexible and process-independent
- Firm Core(Netlist)
- Each type of core has different modeling and test requirements

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Challenges
SOC Test

- System Integrator may have
  - Very limited knowledge of the adopted core
- Core Provider may not know
  - Which test method, what types of faults, and what level of fault coverage to use
- Test of the embedded IP core
  - Joint responsibility of both core provider and system integrator

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IP Core Level Test
SOC Test

- Test Ready Core
  - Ease integration and test reuse
    - Resolve access issues through design recommendations
    - Test architecture flexibility during integration
    - Supply all required test information
- Minimize:
  - Data bandwidth, Volume, Test application time
- IP protection

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Test Access
SOC Test

- No Direct Physical Access Method
  - Test access mechanism is required
- Test Access Mechanism
  - Transports test from source to core and from core to sink
  - Isolates IP core
  - Provides features to test the hardware in between the IP cores

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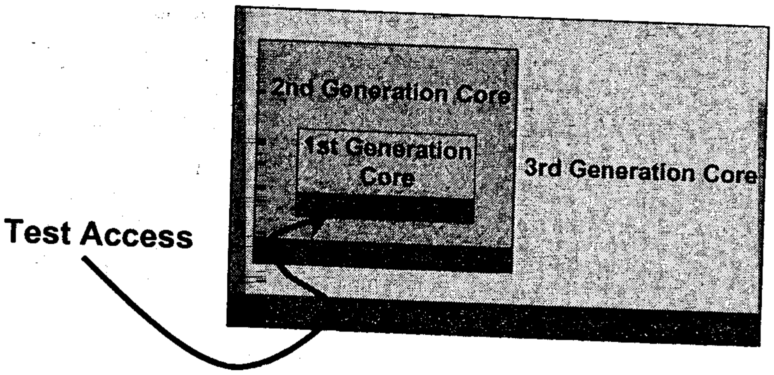
Hierarchical Core
SOC Test

- Today's chip is tomorrow's core



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System-Chip Level Test

SOC Test

- Composite Test
  - Individual test for each IP core, UDL, interconnect logic and wiring
- Test Scheduling
  - To meet SOC requirements such as total test time, power dissipation, area overhead
  - To avoid affecting the initialization and final contents of individual cores
  - sufficient fault coverage, overall test cost, time-to-market

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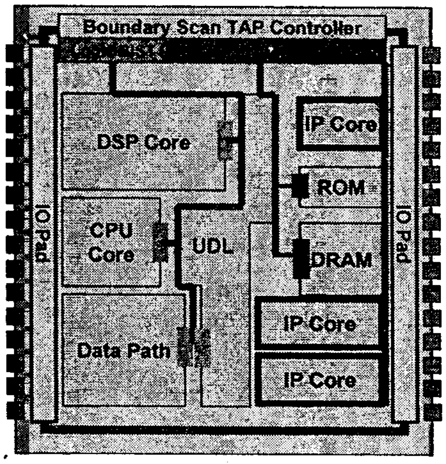
System Level DFT Architecture

SOC Test

- Boundary Scan
- Test Access and Support
- Memory BIST
- Logic BIST



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IEEE P1500 Working Group
SOC Test

- Working toward a standard to facilitate interoperability with respect to testing
  - Not include core's internal test methods
  - Not include chip-level test access configuration
  - Core Test Language(CTL)
    - From core provider to core user
  - Core test wrapper
    - Easy test access of the core in a system chip design

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Delay Test
SOC Test

- Timing Verification of IP-based Design
  - Among the most challenging problems
  - Require delay test, especially path delay test
- Path Delay Test Problems of SOC
  - How to apply two test patterns ?
  - How to handle path delay faults traversing both IP cores and UDLs ?

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Built-In Self Test
SOC Path Delay Test

- Area Overhead
  - BIST for stuck-at should be revamped to generate two test patterns
- Low Fault Coverage
  - Test access mechanism is required to gain fault coverage

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Scan Design
SOC Path Delay Test

- IP Core Test Wrapper
  - IEEE P1500's test access mechanism is based on a variant of boundary scan
  - Wrapper can sensitize only partial paths in IP cores
  - Standard scan register cannot apply two test pattern

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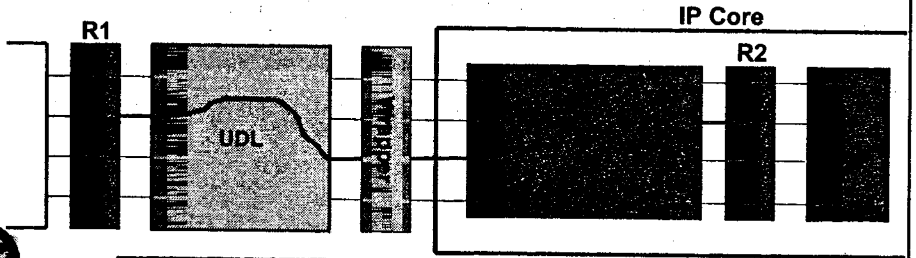
Scan Design

SOC Path Delay Test

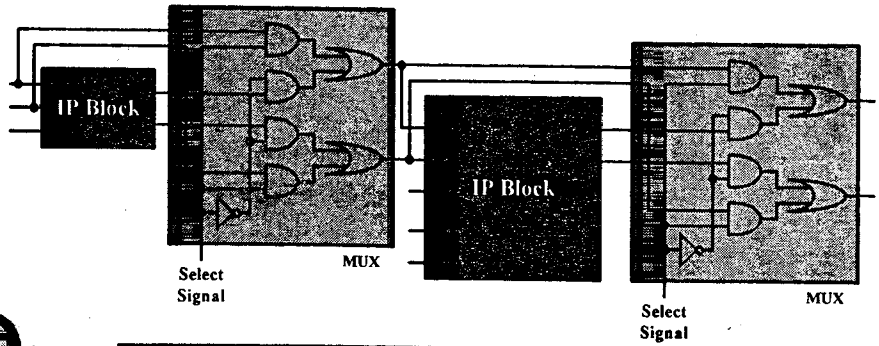
- Single Cycle Path : From R1 to R2
  - R1, R2 can apply two test patterns
    - Enhanced Scan ?
  - Part of wrapper on the path can be transparent



Multiplexing

SOC Path Delay Test

- Test sets of IP provider are applied by the primary ports of SOC through the MUX



Multiplexing

SOC Path Delay Test

- Reduced to the path delay fault testing of each of the IP blocks
- Complete path delay calculation is required
  - Suited to delay evaluation of a prototype SOC
  - Impractical for production testing due to the difficulty of accuracy measuring analog delay values

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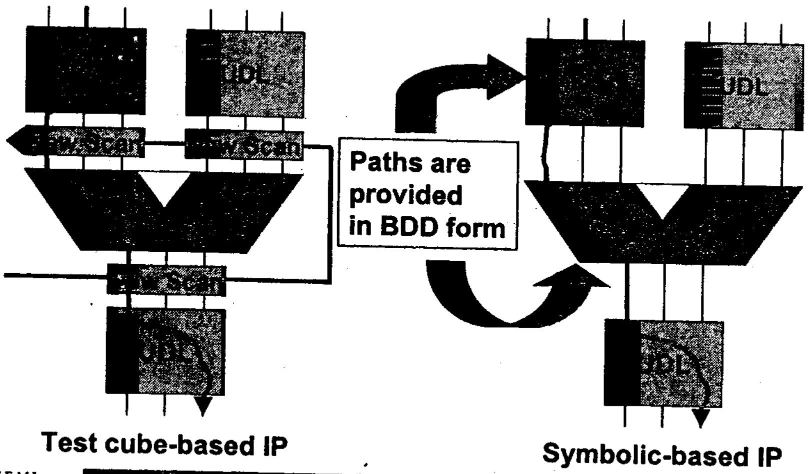
Symbolic Path Modeling

SOC Path Delay Test



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Symbolic Path Modeling

SOC Path Delay Test

- Abstract an IP block's paths in BDD form
  - No extra scan logic
  - Circuit Partitioning to reduce model size
  - Test all testable complete path of SOC
- Impractical to complex circuits
- Symbolic paths of IP core simplify the reverse engineering

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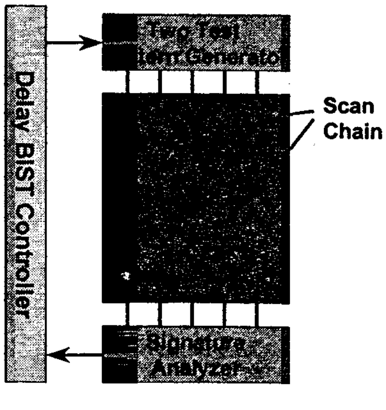
Current Works

SOC Path Delay Test



- Weighted Random Two Pattern BIST
  - Standard scan based design
  - One LFSR(Linear feedback shift register)
  - High fault coverage
- No internal info. required

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Current Works

SOC Path Delay Test

- New Statistical Path Delay Fault Modeling
  - Accurate testability measure
- Efficient Boolean Description an Test of Custom Logic Blocks(CLBs)
  - For IP core provider

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Conclusion

Future challenges

- DFT Methodology of delay test for both IP provider and system integrator
- Methodology for selecting critical path traversing both IP cores and UDL
- Compatible to IEEE P1500
- Test Reuse

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Any Questions?

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