The Split Walking One Sequence for Wiring Interconnects

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Abstract — In the boundary scan environment, the test size should be minimized maintaining diagnostic capability. This paper presents an efficient test approach to the fault detection and the diagnosis of the wiring interconnects and shows how the new test eliminates both the aliasing syndromes and the confounding syndromes.

I. INTRODUCTION

The ever-increasing miniaturization and complexities of electronic circuit have made the testing of the circuit very hard. And the highly comlex packaging technology such as surface mounting and multiple-chip modules has brought the difficulties in the testing of the printed circuit board(PCB) since it reduces the test points or even eliminates them.

Traditionally, manufacturers have been used both in-circuit test and functional test[1]. In the in-circuit test technique, the devices on a board are accessed by *bed-of-nails* -the probes on the ATE, in which the physical contacts with I/O pins are made to the components. But this technique requires very high test costs and causes the back-driven problem. Fucnctional tests are applied to the edge connectors on a board. In this case, the board is considered as a single device. However, the test application cost is very expensive to achieve the acceptable fault coverage to the board. Futhermore, for some product it is impossible to reach the desired fault coverage. To solve these problems, many Built-in Self-Test(BIST) and Design-for-Testabillty(DFT) techniques have been proposed.

A DFT framework performing as the virtual probes was proposed as IEEE standard 1149.1, which is composed of boundary scan chain and test access port[2]. The standarization of the 1149.1 has alleviated the difficulties in the testing by means of increasing the controllability and the observability in each I/O pin. However, due to the serial nature of the scan cells, the use of the scan design techniques leads to the highest application cost since the test data, which consist of the test patterns and the responses, need to be shifted in and out of the circuit serially through a single scan chain. Therefore, to reduce the test application time, it is important to reduce the number of the parallel test vectors for detecting and diagnosing the faults in the wiring interconnects. The problem of the optimal test generation for the wiring interconnects has been extensively studied. The test methods are divided into two type by Kautz[3], i.e., the structural tests that use the information about nets and the behavioral tests that do not use the information. The two types of behavioral test are distinguished from each other by the process of detecting and diagnosing faults[4]. The one-step tests make the fault detection and diagnosis in the wiring interconnects possible by applying a set of test patterns. But to cover all the multiple faults, the number of the parallel test vectors by previously studied one-step algorithm is proportional to the number of the nets. In the multiple-step algorithm, after applying a test for detecting the faulty nets to all the nets, its responses are analyzed and more tests for diagnosing the faults in the faulty nets are additionally applied. But after the test set for detecting the faulty nets is applied, the process of diagnosing its responses makes the test time longer. Also the test size may be larger than the size of the walking sequence if there are many faulty nets in the wiring interconnects.

It is important to test the various kinds of fault between nets such as open net faults, stuck at faults, and AND, OR and dominating type shorted net faults. In this work, we consider the problem of generating a test set which can cover the multiple faults without repair. Also the efficienct test sequence called as *the split walking sequence* is proposed on assumption that both short and open cannot exist in a net and only 2-net shorts exist on the nets. Based on this assumption, the test based on this new algorithm is superior to the previous one-step test sets in that the new test eliminates not only the aliasing syndromes but also the confounding syndromes and the test size is much smaller than the

*This research was supported by Korean Science and Engineering Foundation. (Contract no. KOSEF 96-0102-16-01-3)

walking sequence.

This paper is organized as follows. In the following section, we will describe the fault models and definitions. In section 3, currently known alogrithms are reviewed. And the split walking sequence is presented in section 4 followed by conclusions.

II. Fault Models and Definitions

We assume that there are three types of fault commonly associated with the nets in the wiring interconnects : stuck at fault, stuck open fault and bridging fault. A stuck at fault is modeled when the faulty net is constantly at logical '1'(stuck-at-1) or constantly at logical '0'(stuck-at-0). A stuck open fault is modeled for the floating faulty net at an input. In this case, the input is updated to '1' or '0' dependent on the applied technology. A bridging fault creats a short between two or more nets. This fault is called as *short*. The fault models for the shorted nets can be classified into AND-short, OR-short, and Weak-short. When a fault is modeled as OR-short, the resultant logic value of the bridged nets is an OR of the logic values of the individual nets. Assuming that the resulting behavior of two or more bridged nets is an AND of the logic values of the individual nets, the bridging fault can be modeled as AND-short, when the resultant value is not known but lies between '0' and '1', the fault is modeled as Weak-short.

It is known that the bridging faults between two nets called as *2-net shorts* occur more frequently than the bridging fault between multiple nets called as *multiple-shorts*. And a multiple-short may be considered as a superset of single 2-net shorts. Also the full diagnosis of 2-net shorts makes the probabilities of the confounding syndromes by the multiple shorted nets very low. For these reasons it is considered acceptable if only the shorts between two nets are assumed instead of all the shorts between more than two nets.

The definitions used in this paper are established in [4,5,6]. Some informations are repeated as follows.

Net : the interconnect wiring between the output pins and the input pins of chips or cards.
Test Pattern : the set of logic values which is need to be assigned to each boundary scan cell and card pin.
Paralle Test Vector (PTV) : the vector applied to all the nets of an interconnect network in parallel.
Sequential Test Vector(STV) : the vector applied to a net over a period of time by a number of PTVs.
Sequential Response Vector(SRV) : the response of a net to a STV. STV will differ SRV if there is fault on the net. If the net is fault free, its STV are identical to the SRV applied to the net .
Detection : the ability to detect faults.
Diagnosis : the ability to determine which nets are shorted together or faulty.
Self-Diagnosis: The property of test sequence when every faulty net can be identified by checking its own SRV only.
Syndrome : the SRV of a faulty net when all the nets involved in a short have the same faulty SRV.
Aliasing Syndrome : the resultant syndrome that happens when the faulty response of a set of the faulty nets is the same as a correct SRV of a net not in the set.
Confounding Syndrome : the syndrome that results from multiple independent faults are identical.
OR-Cover : we assume that two vectors: V_i and V_j exist in a set of vectors. V_i *OR-Covers* V_j if V_i has a '1' in every bit where V_j has a '1'.
AND-Cover : V_i *AND-Covers* V_j if V_i has a '0' in every bit where V_j has a '0'. According to the applied technology on a board or a system, the type of *cover* is determined.
Independent : V_i is *independent* from V_j if V_i dose not cover V_j.
Set-cover : Let V_j be the result of an OR of a set of vectors $V_{j_1}, \ldots, V_{j_k}$. A vector V_i set-covers the vectors $V_{j_1}, \ldots, V_{j_k}$ if V_i covers V_j.

III. Review of the Previous Algorithms

The test algorithms can be classified into the behavioral test and the structural test [3]. In this section, the brief review of the previous sequences for testing the interconnects will be presented and we will focus on the previous behavioral test.

Many algorithms have been developed to detect and diagnose the faults in the wiring interconnects. The earliest behavioral algorithm for the behavioral testing was presented by Kautz[3]. The *Counting Sequence* has been proposed to detect all the shorted nets in n nets with $\lceil logn \rceil$ PTVs. If the test vectors are applied through n boundary scan cells, the test time is $n \lceil logn \rceil$. The *Modified Counting Sequence* proposed by Goel and McMahon is the modified form of the sequence of Kautz[7]. The STVs composed of all '1' bits cannot detect the stuck-at-1 on a net. In a similiar fashion, the test vector composed of all '0' bits cannot detect the stuck-at-0. Therefore, Goel and MaMahon excluded these two STVs in a test set of Kautz so that the stuck at faults on all the nets can be detected. However, these two algorithms cannot eliminate the aliasing syndromes. Therefore, the *True/Complement Counting Test Algorithm* was presented by Wagner to avoid the alising[8]. The number of PTVs is $2\lceil logn \rceil$ twice as the number of PTVs by the Counting Sequence. This test can eliminate the alising syndromes but cannot eliminate the confounding syndromes by 2-net shorts or multiple-shorts. The *Walking Sequence* can eliminate both the aliasing syndromes and the confounding syndromes[5] [9]. If there are n nets, after n shifts of the total chain,

the logical '1' or '0' has walked over all the nets. Therefore, the test time is n^2. The advantage of the walking sequence is that it is easy to generate the sequence. The drawback is that the large test set is generated proportional to the square of the number of the nets. The *Maximal Independent Set* was proposed in [4]. In the maximal independent set, if the number of PTV is p, every STV has $p/2$ '0' bits. This algorithm generates the maximum size independent test sets according to the Spener's Theorem. Therefore, this algorithm is good for self-diagnosis. But this method also eliminates the aliasing syndromes but does not eliminate the confounding syndromes by 2-net shorts.

In the following section, we will propose the new test sequence algorithm which eliminates both the confounding syndromes by 2-net shorts and the aliasing syndromes by 2-net shorts or multiple-shorts. Also the property that the SRVs of 2-net shorted nets is independent from each other will be proved.

IV. Split Walking Sequence

We assume that stuck at faults and OR-shorts are modeled in all n nets and multiple independent faults does not exist on a net. The process of generating the new test set is as follows.

First, we define a *group* as a set of nets and a variable k as the value of $\lceil\sqrt{n}\rceil$. All the nets are divided into the groups: G_1, G_2, G_3, ..., G_{N_g}, in which N_g represents the total number of groups. An expression $num(G_i)$ is defined as the number of all the nets in G_i. From $i = 1$ to $i = N_g - 1$, $num(G_i)$ is equal to k. $num(G_{N_g})$ is smaller than k or equal to k: $num(G_{N_g}) \leq k$. And we define $num(G_{N_g})$ as *remainder* R. The total number of the nets n is equal to $(N_g - 1) \times k + R$, in which both the total number of groups N_g and the remainder R are determined. Depending on N_g and R, the nets are divided into N_g groups.

The new test sequence has three types of partial sequence: *nonequal- group sequence* $S_{nonequal}$, *equal-group sequence* S_{equal}, and *distance sequence* $S_{distance}$. First, a walking sequence $S_{nonequal}$ walks '1' over all groups from the lowest bit b_1 to b_k in the STVs of $S_{nonequal}$ in parallel, in which the STVs of the nets in a group are equal and the STVs of the nets in other groups differ. Then another walking sequence S_{equal} is applied across groups, in which the STVs of the ith nets of every groups are equal. Therefore, the PTVs of each group are equal. The logical value '1' also walks over from the lowest bit b_1 to b_k in the STV of S_{equal}. We will introduce the variable *distance* D, which depends on the '1' bit positions in the STV of $S_{nonequal}$ and the STV of S_{equal}. We assume that the distance of the first net in G_1 is 1. In the first net in G_1, the '1' bits exist as b_1 in the STV of $S_{nonequal}$ and b_1 in the STV of $S_{nonequal}$. If in a net, the '1' bit exsits as b_p in the STV of $S_{nonequal}$ and b_q in the STV of $S_{nonequal}$, the D is $p + q - 1$. Finally, one walking sequence $S_{distance}$ is applied to each net. In this case, the D presents the '1' bit position in the STV of $S_{distance}$. By applying to these three partial sequences, the split walking one sequence is composed and applied to all the nets. From the symmetrical point of view the same reasoning is valid for AND-shorts.

Group	Nets	$S_{nonequal}$			S_{equal}			$S_{distance}$			
G1	N1	0	0	1	0	0	1	0	0	0	1
	N2	0	0	1	0	1	0	0	0	1	0
	N3	0	0	1	1	0	0	0	1	0	0
G2	N4	0	1	0	0	0	1	0	0	1	0
	N5	0	1	0	0	1	0	0	1	0	0
	N6	0	1	0	1	0	0	1	0	0	0
G3	N7	1	0	0	0	0	1	0	1	0	0
	N8	1	0	0	0	1	0	1	0	0	0

Table 1: Split Walking One Sequence

A sample set of test patterns by the split walking one algorithm is shown Table 1. Assuming that there are eight nets in the wiring interconnects. k is 3. Also it is easily shown that N_g is 3 and R is 2.

Now, we will show that the split walking sequence detects and disgnoses the stuck at faults and the briding faults. It is clear that the STV for a net has '1' and '0' bit strings and the the test pattern detects and diagnoses the stuck at faults. A STV applied to a net is independent from the STVs in other nets, so that the aliasing syndromes by two shorted nets or multiple-shorted nets can be eliminated. The STVs of the nets in a group are independent from each other. If multiple 2-net shorted nets exist in a group, the SRVs of independent 2-net shorts are independent from other SRVs of other 2-net shorts. When the nets of G_1 and the nets of G_2 are shorted, the SRVs of this 2-net shorted nets is independent from the STVs of other nets in G_1 and the STVs of other nets in G_2. Therefore, the confounding syndromes by two shorted nets can be eliminated.

V. RESULTS

As the large test set is generated, this problem of the test cost is very serious if the boundary scan is builded in the wiring interconnects. The walking sequence which can eliminates the confounding syndromes by 2-net shorts generates n PTVs for n nets. But the split walking sequence produces the test set much smaller than the test set of the walking sequence. For n net if R is equal to k, the number of the nets in any group is also k. And the maximum D is $k + N_g - 1$. Therefore, the number of PTVs is $N_g + k + (k + N_g - 1) = 2N_g + 2k - 1$. If R is not identical with k, the maximum D is $k + N_g - 2$. In this case, the test length is $N_g + k + (k + N_g - 2) = 2N_g + 2k - 2$. For example, if there are 1600 nets in the wring interconnects.

the number of PTVs by the walking sequence is 1600. But the size of the new test is 159. Therefore, it is clear that based on assumption that only 2-net shorts exist in the wiring interconnects, the test size is much reduced compared to the walking sequence.

VI. CONCLUSION

In this paper, we reviewed the previous studied algorithms which are used by the boundary scan environment and addressed the fault models and definitions. Also the reasons why only 2-net shorts are considered were described. By using these addressed fault models and definitions, the efficient test sequence defined as the split walking sequence was presented and the process of the test generation and test time were well explained. The proposed new test sequence detects not only all the faults in the wiring interconnects but also eliminates the confounding syndromes between two nets while the test size is much smaller than the walking sequence. Therefore, this new algorithm makes the interconnect tests very efficient.

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