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AN EFFICIENT BIST ARCHITECTURE FOR BOARDS WITH MULTIPLE SCAN CHAINS *

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Abstract

In the board level BIST(Built-In Self Test) architectures, the test application time is an important factor in view of the test cost. To reduce the test application time, the parallel operational multiple scan chain configuration was proposed. However, it is incompatible to the 1149.1. This paper describes a new efficient BIST architecture for the boa :s with the multiple scan chains in the standard environment. In the new architecture, two scan chains are accessible at a time by one test bus. With this approach, the test application time can be greatly reduced at the small cost of the area overhead.

1 Introduction

The highly complex packaging technology, such as surface mounting and multiple-chip modules, has brought out the extreme difficulties in testing boards since it reduces the test points or even eliminate them. The development of the 1149.1 [1] has alleviated such difficulties by means of increasing the controllability and the observability in each I/O pin. However the use of scan design techniques leads to the highest application cost since test data, which consist of the test patterns and the responses, need to be shifted in and out of the circuit serially through a single scan chain.

To reduce the test application time, there have been many attempts. One of these approaches is to use multiple scan chains [2]. In parallel multiple scan chain design, each scan chain requires its own test port signals. In addition, the 1149.1 does not support the parallel operation of multiple scan chains. In [3], only one scan chain can be accessed at a time. Therefore the interconnect faults among more than two scan chains cannot be tested. In this paper, we propose a new multiple scan chain access algorithm and the board level BIST architecture. In the new approach, the test application time can be greatly reduced due to the simultaneous access of two scan chains.

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2 Algorithm

The proposed approach uses 6 stable states, that is, the Test-Logic-Reset, the Run-Test/Idle, the Shift-DR, the Shift- IR, the Pause-DR, and the Pause-IR states. This is similar to shadow protocol which was proposed in [4] except that the proposed approach uses two additional stable states, the Shift-DR and the Shift-IR states. The configuration of the proposed BIST architecture which can access multiple scan chains is shown in Figure 1. As shown in Figure 1, it consists of eight Chain Link Blocks(CLBs) and a Master Control Block(MCB). As in the system level backplane test [5,6], the connection setup procedure is composed of the broadcasting of the link request and the acknowledge of the connection. The MCB can access a scan chain when each scan chain is in a state among 6 stable states. To access a scan chain, the MCB loads the 8-bit address register, whose bits indicate each scan chain, by setting the corresponding address bit field, and broadcasts the link request signal which consists of the signals as shown in Table 1. In response to the link request signal, each CLB checks whether its own address field in the address register is set or not. If its address field is set, it starts the connection setup

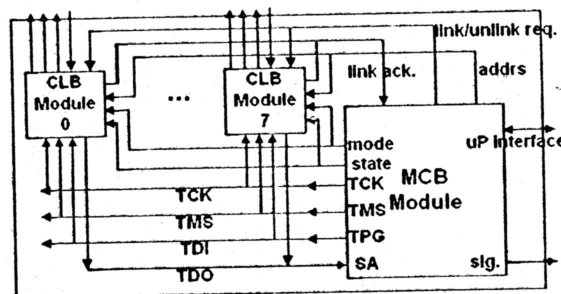

Figure 1: BIST Module for Multiple scan chains

Input Values	Requested Actions
Z	Idle State
1	Link Request
0	Unlink Request

Table 1: Link/Unlink Request Signal

procedure by linking its test port signals to the MCB test bus. After the link procedure is completed, the CLB clears its address field and activates the link acknowledge signal. In response to link acknowledge signal, the MCB checks whether the correct address field is cleared to ascertain the success of the connection setup procedure. When the connection setup procedure is succeeded, the MCB starts the required control operations.

In the new approach, the MCB accesses two scan chains at a time to reduce the test application time. The data scan stages start in the Run-Test/Idle state. In the Run-Test/Idle state, the MCB generates the TMS sequences required for the connected CLB to change its state to the Shift-DR state. After the CLB enters the Shift-DR state, instead of waiting for the termination of the scan shifting stages, the MCB disconnects the CLB which is currently connected. And the MCB tries to connect another scan chain. The scan chain connection and test data shifting operations are the same as the previous ones. However, the particular data transmission and a receiving techniques are required since the test data of the two scan chains must hold one MCB test bus in common. To do this, the new approach uses two scan shifting modes as shown in Table 2. The 1149.1

Mode	Required Actions	Clocking Strategy
A	Test Data Capture	↑ of TCK
	Response Data Transimission	↓ of TCK
B	Test Data Capture	↓ of TCK
	Response Data Transmission	↑ of TCK

Table 2: Scan Shifting Modes

requires the scan-in operations must occur at the rising edge of the TCK and scan-out operations at the falling edge of the TCK. In the mode A, the CLB under test shifts its test data into the ICs at the rising edge of the TCK and shifts out its test responses from ICs to TDO bus of the MCB at the falling edge of the TCK likewise the standard. In the mode B, however, in order to avoid the data collisions, the MCB generates test data for the CLB under test to capture its test data at the falling edge of the TCK. The captured test data are scanned into the ICs at the rising edge of the following TCK clock to operate compatible to the standard. The response data shifted out from the ICs at the falling edge of the TCK are held by disabling the TDO buffer until the next rising edge of the TCK. At the rising edge of the TCK, the response data are transmitted to the MCB TDO bus by enabling the buffer. To compact the correct response data, the MCB requires the specific clocking strategy as shown in Figure 2. The MCB collects the A mode response data at the falling edge of the SCLK, and the B mode response data at the rising edge of the SCLK. The SCLK is shifted a quarter of a period of the TCK. The SCLK is used as enable signals for the signature analyzer registers. After the two scan chains enter the Shift-DR state, the MCB monitors the scan shifting counters which indicate the shift status of the CLBs under test. The MCB reconnects the previous CLB before its scan operations are terminated. As soon as the scan operations are terminated, the MCB makes the CLB to move its state to the Pause-DR state, and disconnects in that state. Now, the MCB connects another scan chain, and repeats the previous operations. In this way, MCB can access two scan chains at a time with only one test bus. After all the CLBs under test enter the Pause-DR state, the MCB connects all the CLBs in the Pause-DR state and makes all the connected CLBs to change their states to the Run-Test/Idle state if there are ICs in the BIST operations. Otherwise, all the connected CLBs move to the next Pause-DR state. In this way, the interconnect test among more than two scan chains as well as the test within a chain can be performed.

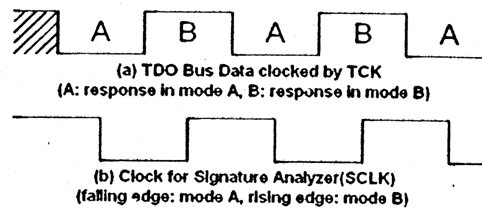

Figure 2: Clocking Strategy for Signature Analyzer

3 Architecture of CLB

The new BIST architecture consists of eight CLB modules and a MCB module. The configuration of the CLB module is shown in Figure 3. The CLB module plays role in connecting its scan chain to the MCB test bus according to the MCB link request signal. Its interface is composed of the IC TAP (ITCK, ITDO, ITMS, and ITDI), the MCB TAP(CTCK, CTDI, CTMS, and CTDO) and the

MCB control inputs(state, addrs, link/unlink req., link ack. and mode). In the mode A operation, the CLB enables the CTDI buffer and connects the ITMS to the CTMS. the mux1 selects the CTDI buffer output, thus the CTDI input can propagate to the ITDO at the rising edge of the TCK as in the standard. The CTDO buffer, however, is enabled only from the falling edge to the next rising edge of the TCK to avoid data collision. In the mode B operation, the CTDI buffer is enabled and the mux1 selects the CREG output whose content is the test input which is captured at the falling edge of the TCK. The CTDO buffer is enabled only from the rising edge to the next falling edge of the TCK. In this period, the test responses which are shifted out at the previous falling edge of the TCK are sent to the MCB TDO bus. After the connection setup procedure is completed, the CLB clears its address field and activates link acknowledge signal. The unlink request signal is activated by the MCB when the access operation ends. In response to the unlink request signal, the CLB checks its current state. To hold the current stable state, the mux2 selects 1 when it is in the Test-Logic-Reset state, otherwise, selects 0.

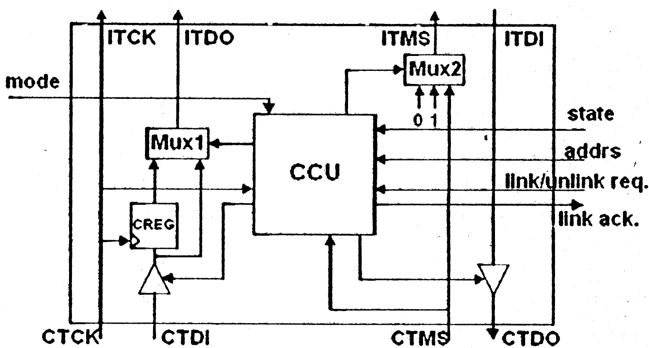

Figure 3: Chain Link Block

4 Performance Evaluations

The new BIST architecture can be evaluated its performances in view of the 1149.1 compatibility, the test application time, and the hardware overhead. These are shown in Table 3.

As shown in Table 3, no additional hardware is required in the single scan design. However, its test application time is excessively too long, so it is unsuitable for the board testing required a large amount of the test data. The parallel operational multiple scan chain design can reduce the test application time. However, the hardware overhead is too large since each scan chain requires its own test port signals and the complex control logics, moreover, it is incompatible to the 1149.1. Therefore it cannot be the solution

	Single Scan Design	Multiple Scan Design (Parallel)	New Architecture
Standard Compatibility	Compatible	Incompatible	Compatible
Required Test Time	Long	Short	Medium
H/W Overhead	No additional H/W required	Large	Small

Table 3: Performance Evaluations of New BIST Architecture

for the testing of the boards in the boundary-scan environment. Our architecture can reduce the test application time since it can access two scan chains at a time. Moreover, the new architecture requires small hardware overhead since the test port of each scan chain hold a master test port signals in common. Our architecture can be the reasonable solution for the cost effective board testing in the boundary-scan environment since it is compatible to the 1149.1.

5 Conclusion

To reduce the test application cost in board level tests, new multiple scan chain access algorithm is developed. Based on the new algorithm, an efficient BIST architecture is implemented. In the new architecture, two scan chains are accessible at a time. This can reduce the test application time in the 1149.1 environment. Therefore the new architecture is desirable for the board level tests.

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