Scan chain swapping using TSVs for test power reduction in 3D-IC

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Abstract

Although the hot issue of chip design becomes 3-dimensional IC, design for testability is still mandatory part of chip design. Scan structure is widely used for system reliability. However, power consumption and heat problems are necessarily considered when design is under test. In this paper, scan chain swapping method using TSVs is presented to reduce shift power in scan in operation. Proper X-filling and swapping algorithm can improve proposed scan chain swapping method. The experiment result demonstrates the power reduction in test mode.

Keywords- through silicon via, power reduction, scan chain swapping

I. Introduction

3D IC technology has become necessary issue because of shorter wire-length and less communication energy. Along with the growth of designing 3D IC, testing for this 3D IC is also important for reliability.

In VLSI design, scan chains are widely used for improving the testability of integrated circuits. Scan flip-flops are connected sequentially to test digital circuits, and this scan design can be also accepted in 3D ICs. However, the test process operation requires more potential power and causes heat problems because of scan-in and scan-out shift operations. When the test mode is activated, test data is shifted into the scan chain. In this operation, transition occurrs when the value of scan flip-flop is changed 0-to-1 or 1-to-0. These transitions can incur power consumption and heat problems. Therefore, to prevent these problems, power reduction techniques in test mode are considered.

The traditional method to lower the power consumption during scan-based test is to reduce the number of scan cells' transitions. There are 2 types of transitions in scan-based test. The shift transition and the capture transition occurr in test operation : capture transition is generated by the difference between scan-in patterns and the corresponding responses, and shift transition is generated by the value of two adjacent scan cells between scan-in patterns. There are some methods to reduce shift power such as don't care bits filling[1], scan chain re-ordering[2], etc.

In this paper, a new scan chain swapping techinique in 3D ICs is presented. The proposed scan chain architecture can propagate signals using not only wire but also TSVs which are used to 3D IC design. And then, these TSVs are used for means of swapping in this proposed method.

The rest of the paper is organized as follow. The proposed sturucture is described in Section 2. And the simulation results are given in section 3. Section 5 summarizes the overall contents of this paper.

II. Proposed Structure

A. Basic Idea

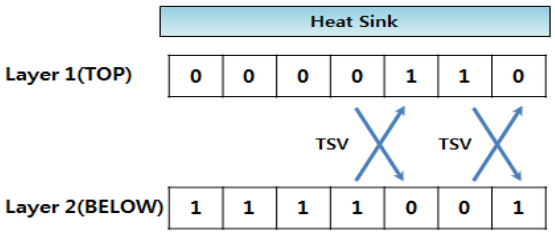

Figure 1. Proposed scan chain re-ordering method

The Fig. 1 shows a conceptual scan chain overview and proposed swapping method in 3D IC design. The scan length of each layer is 7 and different test vectors are shifted into each scan chain. The test vectors of top layer scan chain is "0110000" and those of bottom are "1001111". When these test vectors are inputted each scan chain, flip-flop transitions can be occurred because of shift operation.

To remove these types of transition, scan chain swapping method using TSVs is proposed. Fig. 1 presents the overview of the scan chain swapping method using TSVs. In 3D ICs, TSV can be a way to re-route for scan chain swapping. In Fig.1, fourth scan flip-flop in top layer chain is connected to fifth scan flip-flop in bottom layer. Then, the sixth flip-flop in bottom layer is connected to seventh scan flip-flop in top layer. In this scan chain structures, the TSV that connects fourth scan flip-flop in top layer and fifth scan flip-flop in bottom layer should exist. If the TSV does not exist, new TSV is placed in this site to connect these two scan flip-flops. Using this proposed scan chain swaping method, shift transitions in each layer are reduced. The results are described in Section 3.

B. Filling method

Test patterns have many don't care bits. To test each layer design, these test patterns should be filled with 0 or 1 and this process is called X-filling. In this paper, a X-filling method is proposed to reduce shift power in this scan chain swapping scheme.

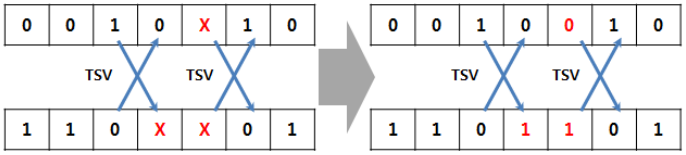

Figure 2. X-filling for proposed scan chain swapping method

Fig. 2 shows the X-filling method for proposed scan chain swapping scheme. There are 3 don't care bits in top and bottom layers. Don't care bit in each layers can be filled with 0 or 1. In this patterns, the best solution for reducing shift power is that don't care bit in top layer is filled with 0 and those of bottom layer are filled with 1. When the part of each scan chain is swapped, this filling algorithm can reduce shift transition in test mode. In the proposed swapping algorithm, all X-values in patterns of two different layers are analyzed and filled with proper values.

C. Swapping algorithm

In order to cover faults in sequential circuits, a lot of test patterns are needed. Therefore, a proper swapping algorithm to swap a part of each scan chain efficiently should be considered. Next pseudo code shows the algorithm for this proposed scan swapping method.

```
Get patterns for top&bottom  layer circuit
Get common pattern num = min(#of_top_pattern, #of_pattern_bottom)
Get common pattern length = min(Top pattern length,  Bottom pattern
length)
Find 0-to-1 and 1-to-0 transition position about all patterns
startPosition_0to1 = max( (#of_transition at i th scan position) * i )
startPosition_1to0 = max( (#of_transition at i th scan position) * i )
if( startPosition_0to1 <  startPosition_1to0 )
  while( k < stPosition_1to0 – stPosition_0to1)
    swap(scan1[k], scan2[k])
else
  while( k < stPosition_0to1 – stPosition_1to0)
    swap(scan1[k], scan2[k])

Perform Low power filling
```

Figure 3. Psedo code for scan swapping method

In this swapping algorithm, a swapping zone should be calculated in a target scan chain. First of all, maximum transition point which are changed 0-to-1 and 1-to-0 among all patterns should be found and determines swapping zone to the length between 0-to-1 and 1-to-0. And then, the swapping zones in each top and bottom circuits are swapped each other. Finally, don't care bits of each scan chain which has swapped part are filled with 0 or 1 according to low power filling method. In this method, transitions in layer which is not adjacent heat sink are priorly considerd. Heat sink adjacent layer is easy to cool down rather than other layers because heat sink can reduce heats through heat sink.

III. Experiment Results

The experiment is conducted using largest ISCAS'89 benchmark circuits and the test patterns that are used in scan in operations is obtained by Tetramax tool. The results shows that shift transition reductions when two different circuits are placed in different layers.

	Circuit	AZ	LP	SS	Comp. with LP
Circuit1	s13207	7,113,415	6,280,687	6,273,690	0.44%
Circuit2	s15850	7,449,462	6,663,703	6,512,352	2.64%
Circuit1	s38417	63,433,526	55,091,982	55,045,511	0.08%
Circuit2	s35932	17,075,512	15,660,351	14,528,669	7.23%
Circuit1	s38584	55,179,779	49,235,123	48,632,167	1.22%
Circuit2	s35932	17,075,512	15,660,351	14,562,039	7.01%

Table 1. Transitions during test mode about each low power methods

Table 1 shows the result of shift transitions in each circuit in each filling algorithm. The terms AZ, LP and SS in first row represent all zero filling, low power filling and proposed scan swapping method, respectively. Proposed scan swapping method can reduce shift transitions as shown in column 5 and column 6 that represents reduction ratio compared with low power filling. In this experiment, firstly, the position of circiut 1 is adjacent to heat sink and circuit 2 is located below circuit 1. Then, the experiment is performed when the position of circuit 1 and circuit 2 is swapped. Column 6 shows reduction ratio when target circuit is not adjacent to heat sink. The object of this experiment is to reduce bottom layer transitions in test mode. Therefore, the transitions in bottom layer is mainly considered. In this result, proposed method can reduce shift transitions in bottom circuit compared with low power and all zero filling methods.

IV. Discussion and future work

In this paper, a new scan chain swapping method using TSVs has been proposed which provides shift transition reduction in scan-in operation. Although the layer which is adjacent heat sink does not have dramatical transition reductions, target layer which is not adjacent heat sink can get transition reductions in test mode. A few number of aditory TSVs and little hardware modification can reduce shift power in 3D-ICs to accept proposed scan swapping method.

Acknowledgment

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References

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