Bit Transmission Error Correction Scheme for FlexRay Based Automotive Communication Systems

[1]Inhyuk Choi, Taewoo Han, and [2]Sungho Kang, *Member, IEEE*
Department of Electrical and Electronic Engineering
Yonsei University
Seoul, Korea
Email: [1]{ihchoi, twhan}@soc.yonsei.ac.kr, [2]shkang@yonsei.ac.kr

***Abstract*— In the FlexRay communication network systems which are configured as a large number of ECUs (Electronic Control Units) and network topologies, the receivers have the different asymmetric transmission delays which cause the transmission errors. As the complexity of the communication network topology in vehicle increases, the asymmetric delay is getting longer. In this paper, the error estimation and correction scheme to ensure the integrity of the signal during operation when the transmission error occurs due to the asymmetric delay is proposed. Simulation results show the proposed scheme can correct the transmission errors effectively in performance.**

Keywords—FlexRay communication systems, bit transmission error, asymmetric transmission delay, error correction

I. INTRODUCTION

Recently, the trend toward replacing the mechanical controls with the electronic devices such as the ECU is significant in the vehicle industry. Also, the electronic devices are designed as the distributed systems which compose complex in-vehicle network. In this reason, a faster and more efficient communication protocol for high-performance is required to transmit and process a lot of information among the devices. The FlexRay communication protocol was developed as standard technology to meet the requirement of safety critical automotive communication. The FlexRay supports two independent transmission channels that are configured as the fault tolerable communication and each channel has a maximum transfer rate of 10Mbps. Also, the FlexRay communication protocol has the time-deterministic data transmission (time triggered protocol) that is described as the static segment, and it also supports the event triggered protocol as the dynamic segments [1].

Existing studies related to using two channels to tolerate transmission errors over the noisy channel in x-by-wire was introduced [3]. However, transmitting the same data simultaneously along two channels restricts a variety of topologies. Especially, the dynamic segment uses channels independently for data transmission. For this reason each channel should have an individual tolerance mechanism for the transmission error. In the vehicle network that consists of a large number of the ECU, the asymmetric delay which is increased according to the growing complexity of the FlexRay topologies becomes the cause of the transmission error in particular.

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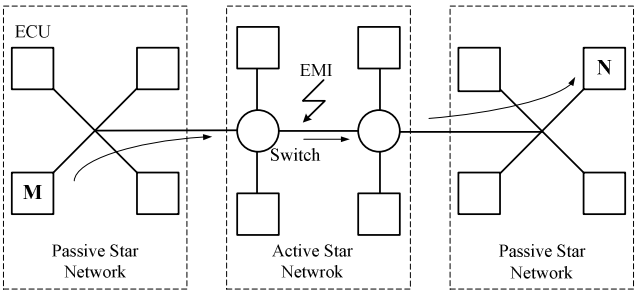

Fig. 1. FlexRay communication system includes active/passive star

The asymmetric delay is caused by the difference between the transfer delays at the rising and the falling edge which is affected by the characteristics of the ECU, the topology type, and EMI (Electronic Magnetic Interference). For example, the asymmetric delay is affected by two ECUs in passive star network, two switches in active star network, and EMI while data is transferred from the ECU 'M' to the ECU 'N' in figure 1. As the complexity of the network topology in vehicle increases, the probability of transmission error occurrence will increase while the asymmetric delay is getting longer. In additional, the asymmetric delay is getting larger according to development of the fine manufacturing process [4]. In this reasons, it makes the network design considering the asymmetric delay more difficult. In this paper, the transmission error correction scheme that estimates the asymmetric delay and the rising edge position in the single-channel operation mode is proposed to ensure the signal integrity. This scheme corrects the transmission error regardless of the variation of the asymmetric delay according to the complexity of the network by simple architecture usage because the rising edge position and the required delay quantity are considered simply.

II. BIT TIMING ERROR MODEL

In ideal case, the number of samples per bit is eight and the sampling cycle duration is 12.5ns according to the FlexRay standard document [1]. The sample count is reset on falling edge of the input signal and the bit value is extracted every fifth sample (sample count is five) that is defined as the strobe point (*cStrobeOffset*=5). Figure 2 presents the transmission

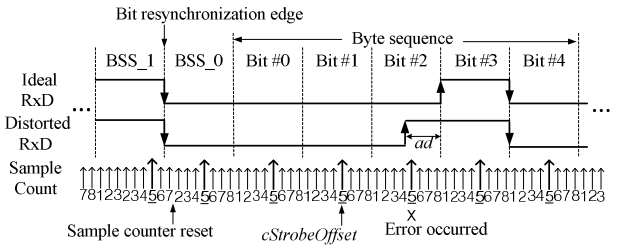

Fig. 2. Transmission error caused by asymmetric delay at Bit #

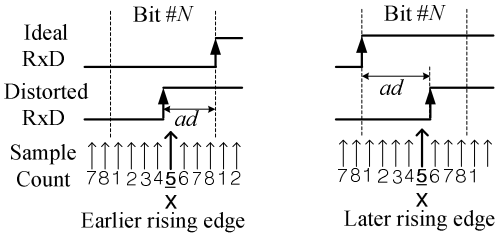

Fig. 3. Rising edge position in transmission error

error which caused by the asymmetric delay (*ad*). In this figure, the rising edge occurred before the expected position by *ad*. So, third strobe in the byte sequence extracts the value of Bit #3 instead of that of Bit #2 by timing interference which exists between Bit #3 and Bit #2.

The rising edge can be occurred earlier or later than expected time by the asymmetry delay. In figure 3, the transmission error will occur when the earlier rising edge located four samples (50ns) apart from expected one or the later rising edge located five samples (62.5ns) apart from expected one. Actually, if two active and two passive star topologies in the FlexRay communication network, an approximately 70ns asymmetric delay may occur when the data between the most distant ECUs is transmitted [2].

III. PROPOSED ERROR CORRECTION SCHEME

Figure 4 represents detect the asymmetric delay length by measuring the number of samples of the HIGH period in the FSS and BSS_1. Each of the FSS and BSS in ideal case of the RxD has eight samples. If 16 subtracted from the measured number of samples denotes positive, the transition is occurred earlier than expected. If the result is negative, on the contrary to this, the transition is occurred later than expected. And the absolute value of the subtraction result is the asymmetric delay *ad*. Because the resynchronization of bit is performed on the

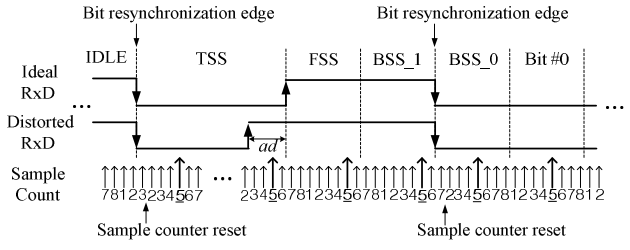

Fig. 4. Asymmetric delay detection at configurable bit sequence

falling edge in the BSS, the falling edges are always present at the same interval in the byte sequence and the transmission error can estimated by the asymmetric delay *ad* and the estimated position of the rising edge.

Figure 5 shows the block diagram of the proposed error correction scheme to compensate transmission errors witch are caused by the asymmetric delay. The samples of distorted RxD are fed the 'edge detection' that analyzes the occurrence of the rising or falling edge by comparing the values of two consecutive samples. The 'asymmetric delay estimation' measures the number of samples from the rising edge between TSS (Transmission Start Sequence) and FSS (Frame Start Sequence) to the falling edge at BSS (Byte Start Sequence). By measuring the number of samples in the section of the HIGH period of the FSS and BSS, the asymmetric delay length and the position of the rising edge are analyzed whether earlier or later than expected one.

If the transmission errors occur as estimated near the rising edge position, the value of bit is corrected by flipping the error bit in 'error correction' Figure 6 shows the detailed description of the 'error correction' in figure 5. The 'bit error estimation' analyzes whether the rising edge position is occurred earlier or later than the expected by the estimated asymmetric delay and its sign bit, then it notifies to the 'edge estimation'. If the 'bit error estimation' forecasts that the bit transmission error can be occurred during the byte sequences, the input for the AND gate becomes HIGH. When the rising edge position is occurred four bits earlier or five bits later than expected position in the byte sequences, the 'edge estimation' inputs HIGH into the AND gate. Consequentially, the value of error bit is flipped then corrected when both inputs of the AND gate become HIGH during the byte sequence. In addition, Figure 7 shows the overall flow diagram of the process of correction for the transmission errors.

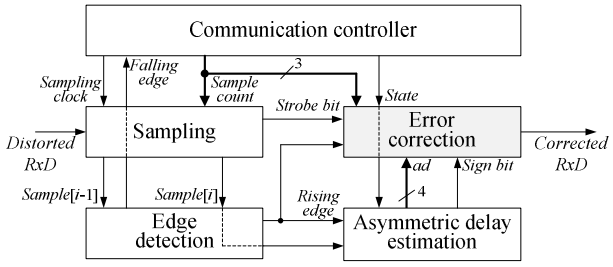

Fig. 5. Block diagram for proposed error correction scheme

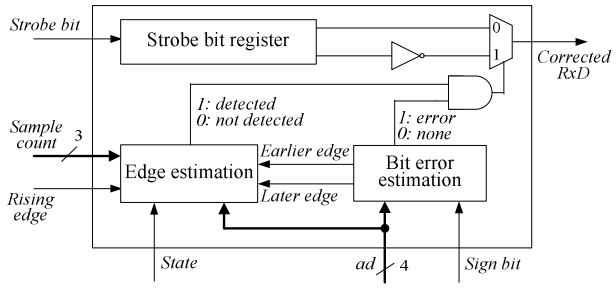

Fig. 6. Detailed description of 'error correction' in figure 5

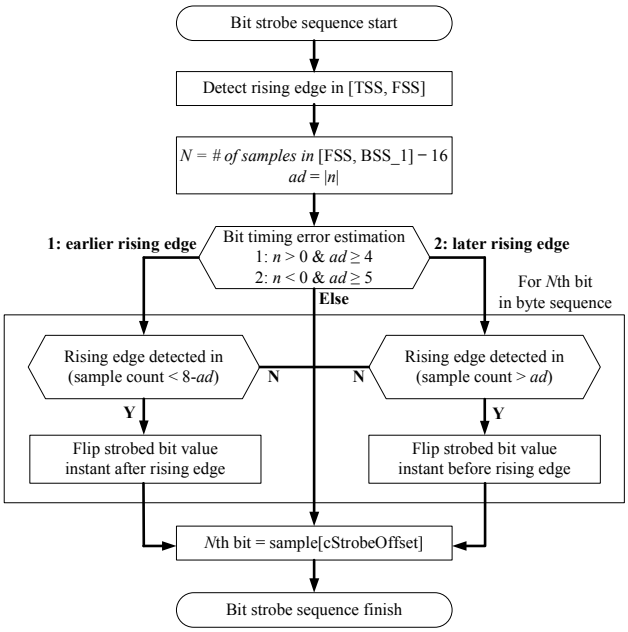

Fig. 7. Flow diagram of error correction scheme

IV. SIMULATION RESULTS

The proposed transmission error correction scheme is implemented using HDL in order to verify it. Figure 8 shows an operational waveform of the proposed scheme. At first, the asymmetric delay is estimated by count the number of samples in the section of HIGH during FSS and BSS (b). Also, the rising edge position is estimated by the asymmetric delay estimation (e). Then, if the strobe bit that the error is occurred and is detected by applying the asymmetric delay estimation and the rising edge estimation in the byte sequence (d), the error bit is flipped and corrected to right bit (f). The result of applying the proposed scheme to the transmission error would perform suitably based confirmation of the error correction. In this case, the operating speed of the proposed scheme satisfies the sampling speed of FlexRay protocol specification [1] and additional hardware for correction is required as shown in Table 1. Because the operational speed is faster than the sampling speed of FlexRay specification, the proposed scheme can be applied to correct the bit transmission error. Additionally, it is expected that the proposed scheme also applied to the requirement of equipment that has faster operational speed than FlexRay. The additional hardware area of the proposed scheme is approximately twice as large as the FlexRay specification which excludes the 'asymmetric delay estimation' and the 'error correction' from the decoding logic. Nevertheless, the proposed scheme has small area compared with the overall FlexRay communication systems.

TABLE I.
COMPARISON IN OPERATIONAL SPEED AND RELATIVE AREA

	FlexRay specification	**Proposed scheme**
Operational speed	80 MHz	190 MHz
Relative area	1	2.2

V. CONCLUSION

As the network topology becomes more complex, the asymmetric delay increases along the transmission path in the FlexRay protocol. And the asymmetric delays at each ECU are different, so analysis of this factor is getting difficult. In this paper, when a transmission error due to the asymmetric delay occurs, the error correction scheme during operation to ensure the integrity of the signal is proposed. Simulation results of the proposed scheme represent that the error correction is effective for asymmetric delay in performance.

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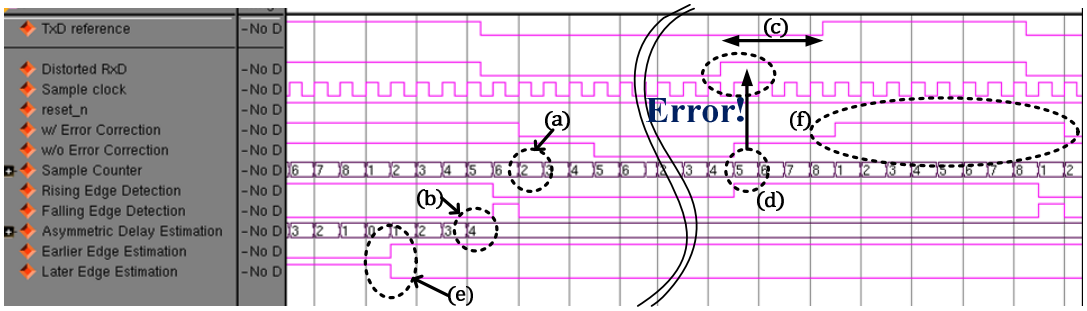

(a) Sample counter reset (b) Asymmetric delay estimation (c) Asymmetric delay
(d) Strobe € Rising edge position estimation (f) Error corrected

Fig. 8. Operational waveform of error correction scheme