Digital Background Self-calibration for High Resolution Analog to Digital Converters

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Abstract

A new self-calibration scheme of a high resolution ADC compensating offset and non-linearity errors is presented. The scheme uses redundant bits of a high resolution ADC for calibrating main characteristic parameters such as offset and non–linearity. The proposed self-calibration circuitry consists of a small adder, a shifter, a subtractor and memory. The experimental results using MATLAB verify the performance of the methodology.

Keywords: analog to digital converters, calibration, offset error, non-linearity error

1. Introduction

Analog to digital converters (ADCs) are widely used in many electronic applications in these days, such as audio recording, wireless communications, video and graphics equipments, and so on. As some appliances have created a need for high speed and high resolution ADCs, self-calibration techniques have been developed to improve linearity of high resolution ADC. This paper presents a new digital background calibration technique to overcome offset and non-linearity errors.

2. Proposed calibration scheme

Using an N-bit ADC does not necessarily mean the ADC has N-bit accuracy. The effective number of bits (ENOB) can be smaller than the actual number of bits. When the ENOB is smaller than the actual number of bits, the resolution of the ADC can be less than the N-bit. The inaccurate bits are considered redundant bits. The proposed method calibrates the ADC using the redundant bits of the least significant bits.

The offset error causes a shift in the analog to digital code transfer curve. The error indicates how well the actual transfer function matches the ideal transfer function at a single point.

To estimate the offset any zero-mean signal is applied to an ADC and then the mean value of the redundant bits output is calculated. The value which means the offset error of the ADC is stored in registers.

The block diagram of the offset error calibration is presented in Figure 1. The offset error calibration block consists of a small adder, a shifter, a subtractor and registers. Using an adder and a shifter the mean value of the least significant bits of the ADC digital output can be calculated. In order to compute the mean value a divider is need but a shifter can be used as a divider when the number of samplings is 2^m where m is a natural number.

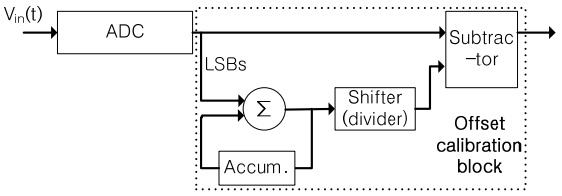

Figure 1: Offset error calibration block

The non-linearity error consists in the not perfect linearity of the ADC characteristics. It is usually measured as the maximum deviance between the real and the nominal characteristics.

Differential non-linearity (DNL) is the difference between each analog increment step and the calculated LSB increment. Integral non-linearity (INL) is the deviation of an actual transfer function from an ideal straight line drawn through the end points. The INL error can be defined as the integration of the DNL. Calibrating DNL error results in calibrating INL error.

The non-linearity error calibration block is depicted in Figure 2. In order to apply the non-linearity correction, DNL should be calculated for each code. To compute the DNL linear ramp signal is applied to the ADC input. When a transition is occurred the content of the timing reference counter is stored in memory. The non-linearity compensation block computes time differences between ideal and actual transition timing and compensates the offset calibrated output. The size of the timing reference

counter is the same as the redundant bits of the ADC. To increase calibration accuracy the counter size can be larger.

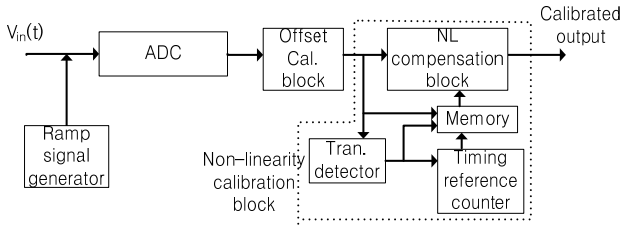

Figure 2: Non-linearity error calibration

3. Simulation results

In order to validate the proposed self-calibration scheme, its performance is evaluated.

A Structural model of a 15-bit pipelined ADC which has 12-bit resolution is designed using MATLAB Simulink. The offset voltage +0.25LSB is inserted to the ADC output, and mismatches are inserted to each stage of the pipeline ADC to make DNL errors. Figure 3 shows the output of the faulty ADC when ramp signal is applied to the ADC input.

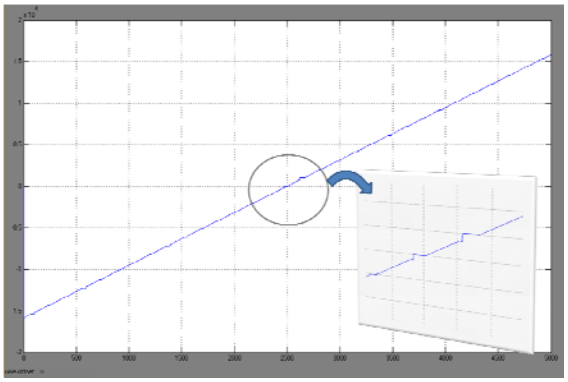

Figure 3: Output of the faulty ADC

The offset calibration scheme using redundant 3-bit is conducted to remove the offset error. Zero-mean small signal of sine wave is applied to the ADC, and the mean value of its least significant bits output calculated from offset computing block is stored in register. The corrected ADC output is generated by subtracting the offset value stored in the register from the ADC digital output. In this simulation, the mean value is computed as '010' according to the offset error.

After the offset calibration, the NL calibration is conducted. A 3-bit reference counter is used to check transition timing. The transition timing information is stored in memory.

The MATLAB simulation result is shown in Figure 4. As a result of simulations, the proposed self-calibration scheme can correct static errors.

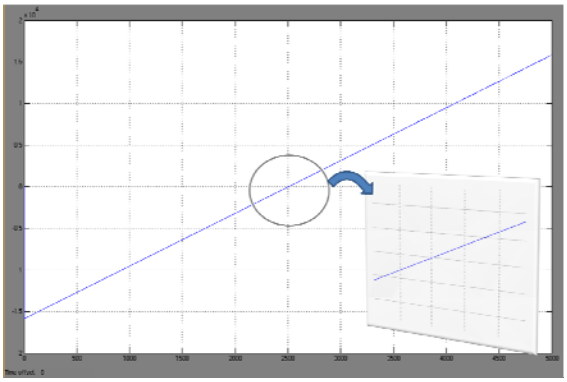

Figure 4: Output of the calibrated ADC

4. Conclusions

A built in self-calibration scheme of high resolution ADC compensating static errors without automatic test equipment is presented. The proposed scheme uses redundant bits of a high resolution ADC for calibrating main characteristic parameters such as offset and non–linearity errors. The offset calibration block has a small hardware overhead only using least significant bits. The non-linearity calibration is simply computed using timing information. Experiments conducted on a faulty ADC have validated the proposed scheme since the built-in self-calibration method can calibrate offset and non-linearity errors. The method may have a delay to get a calibrated ADC output but it does not affect the overall ADC operating frequency and can improve the ADC performance.

References

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