Deterministic BIST Based on a Clustered Reconfigurable Interconnection Network

Dong-Sup Song and Sungho Kang
Dept. of Electrical and Electronic Engineering, Yonsei University,
134 Shinchon-Dong, Seodaemoon-Gu, 120-749 Seoul, Korea
Tel: +82-2-2123-2775, Fax: +82-2-313-8053
dssong@dopey.yonsei.ac.kr, shkang@yonsei.ac.kr

Abstract: In this paper, we propose a new clustered reconfigurable interconnect network BIST to improve the embedding probabilities of random-pattern-resistant-patterns. The proposed method uses a scan-cell reordering technique based on the signal probabilities of given test cubes and specific hardware blocks that increases the embedding probabilities of care bit clustered scan chain test cubes.

1. Introduction

Recently, a reconfigurable interconnection network (RIN) BIST technique that can dynamically change the connections between the LFSR and the scan chain has been developed [1]. However, we can regard test cubes that have many care bits (0 or 1) as random-pattern-resistant-patterns (RPRPs) which make test time long and increase hardware overhead in the RIN BIST. In this paper, we present a new clustered RIN (CRIN) BIST that can enhance the embedding probabilities of RPRPs. This approach is based on a scan-cell reordering technique which exploits the signal probabilities of given test cubes and uses specific hardware blocks to improve the embedding probabilities of reformatted test cubes.

2. Proposed CRIN BIST Scheme

2.1 Basic principles

The embedding probabilities of RPRPs with the LFSR generated test patterns are proportional to the number of Xs of each scan chain cube in the previous RIN BIST scheme. To increase the average number of Xs in the scan chain test cubes, the earlier RIN BIST scheme [1] uses a scan cell reordering method that scatters clustered care bits over all scan chains. However, if 0-care bits and 1-care bits are clustered into separate scan chains, the embedding probabilities of RPRPs can be improved. For convenience, we call the 0(1)-clustered scan chains AND(OR)-Chains and the remaining chains LFSR-Chains. Because care bits in the test cubes are clustered into AND-Chains and OR-Chains, scan test cubes of LFSR-Chains that are fed by LFSR have more X-values than the previous RIN, and thus the embedding probabilities of scan test cubes for LFSR-Chains is enhanced. In the proposed CRIN method, test patterns for AND(OR)-Chains are supplied by an AND(OR) Block which consists of LFSR-tapped 2-input AND(OR) gates. Because the outputs of the AND(OR) Block are weighted by 0(1), the embedding probabilities of 0(1)-clustered AND(OR)-Chains are further improved.

2.2 New scan cell reordering algorithm

This section will explain the development of a new scan cell reordering algorithm based on the signal probabilities of given deterministic test cubes. The proposed scan cell reordering algorithm is implemented by simulated annealing procedures and described in Fig. 1. In this paper, we use the notations represented in Table 1.

Table 1 Definitions of notations

Notation	Definition
m	The number of scan chains
L	The number of LFSR stages
l	Scan chain length
S_i	$0 \le i \le m \times l$, The order of scan cells
T_D	Deterministic test cube set
N_{TD}	The number of total test cubes
N_{AND}	The number of AND-Chains
N_{OR}	The number of OR-Chains
N_{LFSR}	The number of LFSR-Chains

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INPUT : Deterministic pattern set T_D, T_init, T_low, IPT, K_T, Initial scan cell order S_i
OUTPUT : Reordered scan cell S_i', Reordered deterministic pattern set T_D'

Calculate signal probability of each scan cell S_i                    ..... (a)
Reorder scan cells and group AND-chains, OR-chains, and LFSR-chains   ..... (b)
For each group {
   T = T_init ;
   sv = Deterministic pattern set T_D corresponding current S_i ;
   Compute cost C(sv) ;                                               ..... (c)
   while (T > T_low) {
      if (no cost reduction in the last IPT iterations) break ;
      for (i=0; i<IPT; i++) {
         (max, min ) = Find_swap_target(sv) ;                         ..... (d)
         (s_i', sv') = movement(max, min, sv, s_i) ;                  ..... (e)
         Compute cost C(sv') ;
         ΔC = C(sv') - C(sv) ;
         if (ΔC < 0) sv = sv' ; s_i = s_i' ;
         else {
            p = e^(-ΔC/T) ;
            if (random(0,1) < p) sv = sv' ;
            else movement(max, min, sv', s_i') ;
         }
      }
      T = K_T × T ;
   }
}
T_D' = sv' ;
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Fig. 1 New scan cell reordering algorithm

(a) Calculate the signal probabilities P_i of each scan cell S_i using the first one-third of total test cubes where each test cube is sorted in descending order by the number of care bits. Let a deterministic test cube and a test cube set be t_j and $T_D=\{t_1, t_2, ..., t_{NTD}\}$ accordingly. The i-th bit of a deterministic test cube t_j and the signal probability of bit position i are defined as t_{ji}, and P_i, respectively. P_i is calculated by the following equation.

$$P_i = \frac{\left|\{t_j \in T_D \mid t_{ji} = 1\}\right|}{\left|\{t_j \in T_D \mid t_{ji} \neq X\}\right|} \quad for\ 1 \le i \le m \times l \ and\ 1 \le j \le \frac{N_{TD}}{3} \qquad (1)$$

(b) Reorder scan cells according to the P_i in an ascending manner. Also, scan cells that have P_i not exceeding 0.25 form the AND-Chains and scan cells that have P_i exceeding 0.75 form the OR-Chains. LFSR-Chains are made up of the remaining scan cells. For the effect of step (b), 0(1)-care bits can be clustered in AND(OR)-Chains.

(c) The following 'for-loop' performs an operation to scatter Xs over all scan chains. Note that the loop is applied to each group of scan chains (AND-Chains, LF

Table 2 Experimental results for test sets from TetraMax ATPG program (T_{init} = 5.0, T_{low} = 0.1, K_t = 0.97, IPT = 500, $MaxSkipPattern$ = 5000)

Circuit	No. of test cubes	Length of scan chain	No. of scan cells	Previous method[1]					Proposed method							
				No. of configurations	No. of BIST patterns	Storage requirement (bits)	Hardware overhead (percentage)	Encoding efficiency	No. of Configurations	No. of BIST patterns	Scan chain groups	Storage requirement (bits)	Hardware overhead (percentage)	Encoding efficiency	Test time Reduction (percentage)	Storage requirement reduction (percentage)
s5378	1285	7	214	16	257188	272	11.24%	44.54	11	186503	(11, 18, 3)	187	15.05%	64.78	27.48%	31.25%
s9234	1557	8	247	32	517733	544	10.95%	35.55	16	296770	(12, 12, 7)	272	9.20%	71.10	42.68%	50.00%
s13207	3221	22	700	10	205859	170	2.30%	140.20	6	157895	(18, 11, 3)	108	3.59%	220.69	23.30%	36.47%
s15850	3257	20	611	36	588317	612	6.57%	45.71	25	356231	(16, 12, 4)	450	6.50%	62.17	39.45%	26.47%
s35932	7477	56	1763	4	27055	60	0.34%	523.20	3	19983	(17, 13, 2)	45	1.06%	697.60	26.14%	25.00%
s38417	7691	52	1664	243	2065818	4374	17.52%	19.96	133	1225964	(12, 17, 3)	2394	10.54%	36.47	40.65%	45.27%
s38584	12216	46	1464	20	518498	360	1.50%	247.47	8	265469	(9, 19, 4)	144	1.39%	618.68	48.80%	60.00%
Average	—	—	—	52	597210	913	7.20%	150.95	29	358402	(14, 15, 4)	514	6.76%	253.07	35.50%	39.21%

SR-Chains, and OR-Chains). So, the exchange of two scan cells can take place in a group and the net signal probability of each group is not changed. Let the number of specified bits in a j-th scan-chain test cube of an i-th test cube be sp_{ij}. The cost function $c(sv)$ is calculated by the following equations.

$$ave_i = \frac{\sum_{j=1}^{m} sp_{ij}}{m} \quad for\ 1 \le i \le N_{TD} \tag{2}$$

$$dis_i = \frac{\sum_{j=1}^{m} (sp_{ij} - ave_i)^2}{m-1} \quad for\ 1 \le i \le N_{TD} \tag{3}$$

$$c(sv) = \frac{\sum_{i=1}^{N_{TD}} \sqrt{dis_i}}{N_{TD}} \tag{4}$$

(d) To reduce the cost of $c(sv)$, find two scan cells of which the position will be exchanged. Let a scan test cube that has the maximum value of sp_{ij}-ave_i be B_{max} ($1 \le i \le N_{TD}$, $1 \le j \le \alpha$), and let a scan test cube that has the minimum value of sp_{ij}-ave_i in the same test cube as B_{max} be B_{min}. Note that α is N_{AND}, N_{LFSR}, and N_{OR} for the AND-Chain group, the LFSR-Chain group, and the OR-Chain group respectively. The *maximum* is the bit position of a scan cell S_k corresponding to t_{ik}, where t_{ik} is any care bit in B_{max}, and the *minimum* is the bit position of a scan cell S_k corresponding to t_{ik}, where t_{ik} is any X-bit in B_{min}.

(e) Swap the position of two scan cells derived from step (d), and obtain the reorganized scan chain configuration S_i' and the reformatted deterministic test cube set T_D'.

2.3 Logic BIST architecture

Fig. 2 describes the hardware architecture of the proposed logic BIST. The RIN blocks consist of multiplexer switches and they can be reconfigured by applying appropriate control bits to it through the inputs D_0, D_1, ..., D_{g-1}. The parameter g refers to the number of configurations used during a BIST session and it is determined using a simulation procedure. Test patterns for AND(OR)-Chains are supplied by the AND(OR) Block which consists of LFSR-tapped 2-input AND(OR) gates, and test patterns for LFSR-Chains are fed by the LFSR. Because the outputs of the AND(OR) Block are weighted by 0(1), the embedding probability of 0(1)-clustered AND(OR)-Chains can be improved. The control inputs D_0, D_1, ..., D_{g-1} are provided by a d-to-g decoder, where $d = \log_2 g$. A d-bit configuration counter is used to cycle through all possible 2^d input combinations for the decoder. The configuration counter is triggered by the BIST pattern counter, which is preset for each configuration by the binary value corresponding to the number of test patterns for a given configuration.

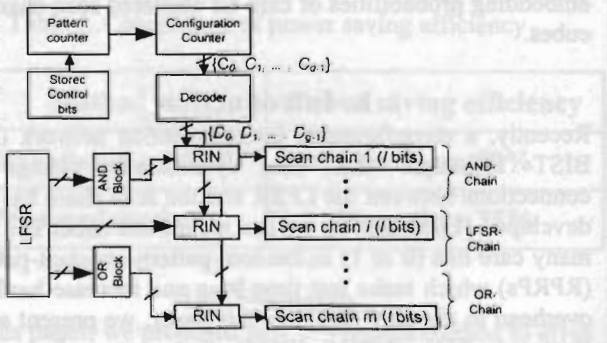

Fig. 2 Proposed logic of the BIST architecture

3. Experimental Results & Conclusion

In this section, we demonstrate the efficiency of the proposed CRIN BIST for the ISCAS'89 benchmark circuits. The set of test cubes used in experiments is obtained from Synopsys' TetraMax ATPG program without dynamic compaction, and by targeting all the single stuck-at faults. Table 2 presents the results where each of the circuits contains 32 balanced scan chains. To limit the testing time, a *MaxSkipPattern* parameter which is defined as the largest number of pseudo-random patterns that are allowed between the matching of two deterministic test cubes is set to 5000. The 'No. of configurations' column shows the total number of configurations needed to embed T_D. And, the parenthesized numbers in the 'Scan chain groups' column are the number of AND-Chains, LFSR-Chains, and OR-Chains respectively obtained from the proposed new scan cell reordering algorithm. The encoding efficiency means the ratio of the number of specified bits in the test set to the amount of storage needed.

This paper presents the clustered reconfigurable interconnect network BIST for the generation of deterministic test cubes. The proposed method offers an attractive solution to the problem of achieving complete fault coverage and short testing time with relatively low storage and hardware overhead.

References

[1] L. Li and K. Chakrabarty, "Deterministic BIST Based on a Reconfigurable Interconnection Network," *Proc. of IEEE Int. Test Conf.*, pp.460-496, 2003