DTMW: Duplicated Transition Monitoring Window for Low Power Test based on Pseudo-Random BIST

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Abstract - This paper presents an improved low power BIST TPG scheme. It is based on the transition monitoring window (TMW). The TMW represses transitions of patterns using the k-value which is the standard that is obtained from the distribution of the TMW to observe over transitive patterns causing high power dissipation in a scan chain. We proposed that the modified TMW structure using duplicated TMW (DTMW) structure. Experimental results show that the proposed DTMW can reduce scan transition by about 60% with improved fault coverage compared to the TMW in ISCAS'89 benchmark circuits.

Keywords: Pseudo random built-in self test, Test generation methodology, Low power design

1. Introduction

A linear feedback shift register (LFSR) is commonly used as a test pattern generator (TPG) in the low overhead Built-in Self Test (BIST). However, because a circuit under test (CUT) may contain many random pattern resistant faults, achieving high performance with pseudo-random patterns generated from an LFSR often requires unacceptably long test sequences [1]. Test patterns generated from an LFSR are less correlative than those produced by normal operation. Therefore, when test patterns are applied to a scan chain, there may be excessive switching activity due to low correlation between consecutive test patterns would dissipate more power [2]. When the peak power exceeds the capability that can be tolerated in a circuit, the circuit during test application would be permanently damaged by excessive heat dissipation. So, a peak power problem due to over-transitive patterns generated from an LFSR is a necessary consideration in a BIST scheme [3]. Several techniques have been proposed to address this problem. A BIST strategy called dual-speed LFSR [4] was proposed to reduce overall switching activities of circuits. It consists of two LFSRs, a slow LFSR and a normal-speed LFSR. However, this will increase test application time. In order to reduce the test length and average power simultaneously, Zhang and Roy proposed a low power random testing technique [5], in which both signal probabilities and activities at the primary inputs are optimized, and both the average power and the test length are reduced significantly. For ISCAS benchmark circuits, while the average of power reduction by using DS-LFSR is 19%, the average of power reduction by using the low power random testing technique in [5] is as high as 78%. The previous techniques are unable to reduce the peak power, since the instantaneous power is not directly related to the average signal activities A new approach was developed to reduce scan shifting transition using a transition monitoring window (TMW) [6]. The duplicated transition monitoring window (DTMW) adopted one more transition monitoring window to observe the original TMW. Because of the TMW size, the region of lower transition density in the TMW should be repressed in spite of dropping the fault coverage. Therefore, the DTMW tried to solve the side effect of the TMW by implementing the iterative clock feeding method based on the transition tendency information which sent from the duplicated TMW.

The rest of this paper is organized as follows: Section 2 introduces notations used in the paper and the distribution of random pattern transitions. In Section 3, it is discussed how the optimal k-value and the TMW size could be set. In Section 4, we propose the duplicated TMW structure that makes improved fault coverage while showing similar power reduction. In Section 5, experimental results are reported for ISCAS' 89 benchmark circuits.

2. Distribution Characteristic of Pseudo-Random Pattern Transitions

We define a "test pattern" as one entire set to fulfill a scan chain and a "vector" means one set of bitwise elements making a test pattern. When a test vector sequence put into a scan chain, a "$S_i(v)$" is defined as one of test vectors that is applied to a scan chain at time i, also a "$S_j(v)$" means consecutive vector of a $S_i(v)$, exactly one of test vectors that is applied to a scan chain at time j. Therefore, when $S_i(v)$ and $S_j(v)$ are different, we call it a transition. This transition becomes a "transition factor" which makes transitions during scan shifting in test mode. If a transition has occurred, then the "pattern transition" gains 1. By using these definitions, we can calculate the pattern transition of each pattern that generated from an LFSR. As a result, we were able to know the distribution of pattern transitions which satisfy pseudo-random Gaussian distribution. Figure 1 shows the pattern transition distribution graph of 5000 test patterns generated from s38584 that has 1452 scan inputs. In the figure, the total number of patterns that has 700 pattern

transitions is about 4000 among 5000 patterns. And the total number of patterns that has 720 pattern transitions is about 4100 among 5000 patterns. So the graph is made by connection of the relation to between pattern transition and pattern number.
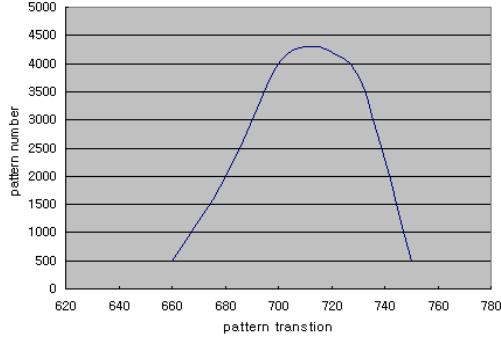

Figure 1   Pattern Transition Distribution Graph (s38584)

We know that *n* scan inputs circuit has maximum *(n-1)* pattern transition factors. When test patterns are generated from an LFSR, some of them would form transition factors. At this time, each transition factor becomes the element of pattern transition. From the relation between the transition factors and the pattern transition, we assumed that the average pattern transition of a pattern would be roughly *(n-1)/2*. Because patterns are generated by a pseudo-random method, we deduced that some rules must exist. This deduction could be observed from graphs of Figure 1. The graph of generated patterns makes an almost symmetrical curve whose central axis is almost *(n-1)/2*. Practically, when we generate 5000 test patterns from s38584, the average pattern transition are 725.3 which are similar value to *(n-1)/2*. This fact can be seen in another ISCAS' 89 benchmark circuits.

Table 1   Comparison between Average Pattern Transition and (n-1)/2 in Some Benchmark Circuits

circuit	average pattern transition	(n-1) / 2	scan inputs
s838	22.77	15.5	32
s1432	36.5	36.5	74
s9234	113.6	113.5	228
s13207	334.2	334	669
s38417	817.4	817.5	1636
s38584	725.3	725.5	1452

Six ISCAS' 89 benchmark circuits are compared for two parameters, average pattern transition and *(n-1)/2*. As we can see from the table, the two parameters generate similar values. That means we can use *(n-1)/2* as the standard for predicting the average pattern transition of circuits. From the distribution characteristics that come from the random pattern property that is generated from an LFSR, we could control average pattern transition of

circuits. This means that if we can have the scheme to monitor the transitive tendency of an LFSR, some over-transitive patterns could be repressed by applying the last scan input vector again. This scheme is the transition monitoring window (TMW). By the TMW, we can achieve a reduction for scan shifting transitions as well as pattern transitions.

3.   Decision to Set Optimal *k-value* and Transition Monitoring Window Size

In Section 2, we have found that pattern transitions are distributed around *(n-1)/2*. The standard acts to make dropping the average pattern transition. In order to set the standard, called a *k-value*, we have to decide how the transitive tendency will be observed. It is accompanied with the transition monitoring window (TMW). The TMW is a part of an LFSR. As transitions in a TMW exceed the *k-value*, a vector directed to output is converted to the high correlation vector which is the last input vector in a scan chain. In this paper, we increase or decrease *k-values* to find an optimal transitive repression values. Let us discuss how a TMW size should be selected. Once a TMW is set, the TMW block could observe whole transitions of the LFSR. Therefore, transitions that exceed the *k-value* will be repressed by a MUX. However, we should make the exact definition for the size of the TMW. Experiments were done using 3/4, 1/2, 1/4 of an LFSR size. As a result, a half of an LFSR size was examined as an optimal size for the TMW because of the trade-off between fault coverage and transition reduction. As the TMW size is set to a half of an LFSR size, we should decide how many transitions repress using a *k-value*. Equations (1) and (2) represent formal expressions of the TMW size and the *k-value*.

$$TMW\ size = \frac{LFSR\ size}{2} \tag{1}$$

$$k-value = \frac{TMW\ size - 1}{2} \pm \alpha \tag{2}$$

In order to find the optimal *k-value*, we examined the relationship between various *k-values* and the change of the fault coverage in experiments. As a result, we could achieve about 25~79% scan shifting transition reduction. However, we should give attention to the k-value which is obtained by $\alpha = +1$, because the optimal fault coverage and transition reduction can be achieved simultaneously in that condition. Figure 2 shows graphs for the relation to various α factors and TR and FC. TR is defined as the number of transitions for modified patterns divided by the number of transitions for the original patterns from the LFSR. FC means fault coverage for the modified patterns. In Figure 2 (a), when α factor gets smaller and smaller, we can see that TR tends to improve. Small α factors make longer repressed regions in patterns. Therefore, it can not but improve transition reduction. However, small

α factor makes the decrease of FC in Figure 2 (b). Moreover, when α is smaller than '+1', the slope of the graph is decreased dramatically.

(a) Graphs for the relation between factor and TR

(b) Graphs for the relation between factor and FC
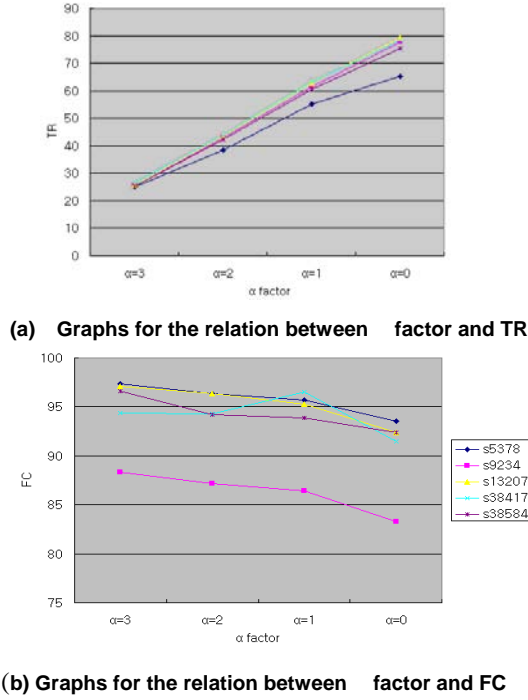
Figure 2 Graphs for various factors according to the change of TR and FC

4. Adoption of the Duplicated TMW

The TMW cannot but observe transitions in the defined range. In Figure 3, the TMW size is set to a half size of an LFSR. If the transition number exceeds the *k-value*, the TMW would repress the outgoing vector to S_{in} until over-transitive region is eliminated. But if the transition density of A is higher than that of B, low-transitive region of B would be repressed by A. It is not a desirable thing because it can impact on the fault coverage.
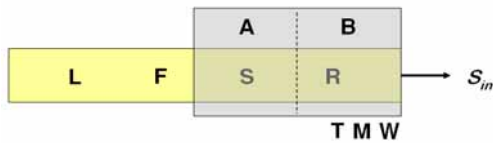
Figure 3 Problem for transition density in the TMW

Therefore, we modified the original TMW to improve the performance. We adopted a duplicated TMW (DTMW) to observe the transition tendency of the TMW. Even though the transition number of the TMW is over *k-value*, the DTMW could keep alive vectors that desired not to repress. The DTMW has its own standard, *d-value*. If transition number of the DTMW is below the *d-value*, transition factors in region B, DTMW region, would not be repressed using clock feeding. Clock feeding is controlled by the size of the DTMW.

$$DTMW\ size = \frac{TMW\ size}{2} \qquad (3)$$

$$d - value = \frac{k - value}{2} - 1 \qquad (4)$$

Because the transition distribution tendency that generated from an LFSR has the regular form following the pseudo Gaussian distribution, DTMW size is set by the same method of the TMW [6]. The *d-value* is the standard for not repressing vectors. Therefore, it should be set by considering the transition balance between the left side of the TMW and the DTMW side. For example, if we have a 32-bit LFSR, the TMW size would be 16 bits. And the *k-value* is 8 by (2) when α =+1 which is the optimal value that mentioned in Section 3. The DTMW size will be 8 bits. In here, the left half side of the TMW has 7 T_f and the DTMW has 7 T_f as shown in Figure 4. The DTMW is operated while the TMW is enabled and transition number of the DTMW should be smaller than the half left side of the TMW.
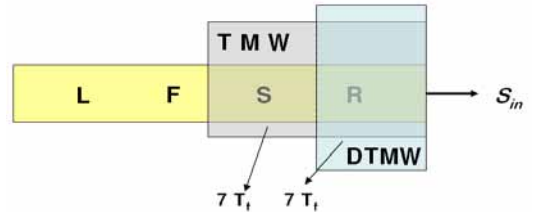
Figure 4 Transition factors after adopting the DTMW

Therefore, *d-value* is determined below the half of *k-value* like Table 2. Exactly, *d-value*=3 is the best value for the DTMW in 32-bit LFSR which could be obtained by equation (4). The left column is in the TMW side, and *d-value* is in the DTMW side.

Table 2 Best value for the *d-value* in the DTMW

The left half of the TMW	*d-value* (DTMW)
4	4
5	3
6	2
7	1

If the transition number of the DTMW is below the *d-value* during the TMW is enabled, pattern shifting clock would be fed until vectors of the DTMW is entirely updated to new vectors from the half left side of the TMW. From this method, we could keep alive vectors that have low transition density that compared with the other side of the TMW. It can help to improve the fault coverage while keeping similar transition reduction performance.

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5. Results

Experiments were conducted using chosen circuits that have many scan inputs among ISCAS'89 benchmark circuits. The proposed approach was implemented by C++ language like the original TMW. We fixed the applied pattern number to 5000. The LFSR sizes to set the TMW sizes are 32-bit, 24-bit, and 16-bit. The TMW size as mentioned is a half of an LFSR size which was determined by additional experiments not shown here. The DTMW size is set form equation (3). We applied the *k-value* when $\alpha = +1$ and the *d-value* were determined by equation (4).

Table 3   Results of the application of various LFSR, TMW, and DTMW sizes

circuit	Pseudo-random fault coverage	32-bit LFSR/16-bit TMW/8-bit duplicated TMW			
		TMW		DTMW	
		TR (%)	FC	TR (%)	FC
s5378	96.27	55.2	95.70	54.8	97.27
s9234	93.36	61.4	86.40	58.8	90.10
s13207	97.83	62.9	95.31	60.2	97.42
s38584	98.41	63.3	96.53	62.5	97.38
s38417	98.47	60.4	93.84	57.9	95.55
circuit	Pseudo-random fault coverage	24-bit LFSR/12-bit TMW/6-bit duplicated TMW			
		TMW		DTMW	
		TR (%)	FC	TR (%)	FC
s5378	96.27	55.3	95.70	54.3	97.40
s9234	93.36	64.4	86.40	61.9	90.15
s13207	97.83	62.9	95.31	60.5	97.33
s38584	98.41	63.3	96.53	62.7	97.48
s38417	98.47	62.2	93.84	61.3	94.49
circuit	Pseudo-random fault coverage	16-bit LFSR/8-bit TMW/4-bit duplicated TMW			
		TMW		DTMW	
		TR (%)	FC	TR (%)	FC
s5378	96.27	65.2	95.04	64.10	97.57
s9234	93.36	68.5	86.24	66.52	90.24
s13207	97.83	63.2	95.63	61.30	97.45
s38584	98.41	63.3	93.45	62.40	97.66
s38417	98.47	64.3	92.68	62.64	94.30

Table 3 shows the results from applying variable sizes of an LFSR, TMW, and DTMW. We were able to achieve an average of 62.4% scan shifting transition reduction in the TMW when $\alpha = +1$. When the DTMW scheme is adopted, the transition reduction was decreased very slightly. As shown in Table 3, we could achieve an average of 60.8% scan shifting transition reduction, which is reduced about 2% compared to the original TMW scheme. However, we should give attention to the change in the fault coverage. Though the repressed region is decreased, vectors that are not repressed are kept alive. This leads to positive impact on the fault coverage because not-repressed vectors made the probability to detect different kinds of faults high. As a result, we could achieve about 2~4% fault coverage improvement. Figure 5 shows the comparative results of the TMW patterns and the DTMW patterns. The shaded box of the TMW pattern stands for one of the repressed regions. Because the TMW observe transition tendency in range of the TMW size, the repressed region would be long. However, the shaded box of the same region for the DTMW shows that the repressed region has changed to its not-repressed vectors. It means that the DTMW patterns have higher probability for detecting faults than those of the TMW.

(a) TMW patterns

(b) DTMW patterns

Figure 5   Comparison the TMW patterns with the DTMW patterns

6. References

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