An Efficient Scan Chain Diagnosis Method Using a New Symbolic Simulation

Sunghoon Chun, Yongjoon Kim, Taejin Kim and Sungho Kang
Department of Electrical and Electronic Engineering Yonsei University
134 Shinchon-dong Seodaemoon-gu, Seoul, Korea
Tel.: +82-2-2123-2775, Fax.: +82-2-313-8053
E-mail: <schun, ykim, tj2010, sshkang> @yonsei.ac.kr

Abstract
Locating the scan chain faults is very important for dedicated IC manufacturers to guide the failure analysis process for yield improvement. In this paper, we propose a new symbolic simulation based scan chain diagnosis method to solve the scan chain diagnosis resolution problem as well as the multiple faults problem. The proposed method uses a new symbolic simulation with the faulty probabilities of a set of candidate faulty scan cells in a bounded range and to analyze the effects caused by faulty scan cells in good scan chains. In addition, we use the faulty information in good scan chains that are not contaminated by the faults while unloading scan out responses. In addition, a new score matching method is proposed to effectively handle multiple faults and to improve the diagnostic resolution by ranking the candidate scan cells in the candidate list. Experimental results demonstrate the effectiveness of the proposed method.

Keywords – Scan chain based test, Diagnosis, Symbolic Simulation

1. Introduction
Scan chain fault diagnosis is the process of identifying the defective scan cell in a scan chain. Several methods have been proposed to diagnose scan chain failures. Previous scan chain fault diagnosis methodologies are classified into two categories. The first category is hardware-based methods [1-4], which needs hardware modification beyond the basic scan design through special scan cell design or additional circuitry. These special designs are then used to facilitate the scan chain diagnosis process. However, these techniques may not be acceptable because of their area overhead, performance penalty and occurrence possibilities of other faults caused by additional circuits.

The second category is software-based diagnosis method [5-11]. Since these scan chain fault diagnosis techniques do not need any modification of the original scan chain design, these techniques are more widely adopted than the hardware-based fault diagnosis methods. The software-based scan chain diagnosis approaches developed previously [5-11] treated the diagnosis as a sequence of guess-and-verify operations. They enumerate a large number of potential candidate faults to search for one that can exactly or partially reproduce the faulty response observed at the outputs of the circuit under test. However, these approaches still produce a large number of candidate lists and low diagnosis resolution. Some previous diagnosis methods [3-8] cannot handle the diagnosis problem if multiple faults are in the same scan chain.

To deal with this problem, several researches have been conducted [9-10]. However, since these methods [9-10] inject one fault at a time on the faulty scan chain and search the most matching candidate based on ranking scores or probabilities, they are still time consuming. In addition, as shown in the experimental results in [9-10], the fault simulation based on algorithms for their techniques cannot achieve high diagnosis resolution for multiple faulty scan cells.

In this paper, we propose a new symbolic simulation (SF-Symbolic simulation) based scan chain diagnosis method called the SF-Sym to solve the scan chain diagnosis resolution problem for a single fault as well as multiple faults. The basic idea of the SF-Sym is to use a new symbolic simulation with the faulty probabilities of a set of candidate faulty scan cells in a bounded range and to analyze the effects caused by the faults of the faulty scan cells in good scan chains. In addition, we use the faulty information in good scan chains that are not contaminated by the faults in the faulty scan chain while unloading scan out responses. Since scan cells in current full scan digital circuits which have millions of gates can take up as much as 30% of the silicon area, most full scan circuits consist of multiple scan chains not a single scan chain to reduce the test application time and to test the combinational logic more efficiently. Therefore, we use the information in other good scan chains except the faulty scan chains to diagnose not only a single fault but also multiple faults in a faulty scan chain.

2. Pre-process of the SF-Sym Diagnosis
The proposed scan chain diagnosis method, called the SF-Sym, consists of four procedures: (1) flush test, (2) the generation of the candidate scan cell window, (3) the SF-Symbolic simulation and (4) the identification of candidate scan cells using the results of the symbolic simulation. The procedure (1) and (2) generate a coarse diagnosis resolution within a short time as the pre-process of the proposed scan chain diagnosis method and the remaining procedures using the SF-Symbolic simulation are for a fine grain scan chain diagnosis resolution (the post-process of the SF-Sym).
2.1 Flush Test

To determine the faulty scan chain and the fault types in the faulty scan chain, flush test patterns which are special test patterns used in [8] are applied in this paper. These flush test patterns were used to differentiate the behaviors of different fault models. Therefore, flush patterns can identify the faulty chains and fault types. In this paper, faults are categorized into three groups: stuck-at faults, transition faults and hold time faults.

2.2. Generating the Candidate Scan Cell Window

To make the candidate scan cell window, it is necessary to calculate the upper bound of candidate faulty cells. The calculation of the upper bound to generate the candidate scan cell window in this paper is focused on reducing search spaces for the scan chain diagnosis using a new simulation presented in next section as a coarse grain procedure.

The concept of determining upper and lower bounds was well established in [7]. We simply use the upper bound calculation method to generate the candidate scan cell window.

To simplify the explanation of the proposed diagnosis method, we use the following definitions.

Definition 1: (Simulation Response) The simulation response of a scan chain is the value combination of the flip-flops after the logic simulation with a given pattern.

Definition 2: (Observed Response) The observed response of a scan chain is the scanned out version of a simulation response. For fault-free circuit, it is equivalent to the simulation response. Note that this is the simulation response in which the fault effects of the faulty scan chain are considered.

Definition 3: (Faillog Response) The faillog response of a scan chain is the observed response of a faulty scan chain in a chip. Note that this is not the simulation response and is obtained from the ATE.

Definition 4: (Snapshot Response) The snapshot response of a scan chain is the value combination of the flip-flops at a certain time instance in the CUT. However, the snapshot image of a scan chain in a failing chip is not actually available because we do not know the real defect location of the scan chain.

After determining the faulty scan chain and the fault type in the faulty scan chain by flush tests, we use logic simulation with a ATPG pattern or a pseudorandom patterns to calculate the upper bound. Note that α is the number of patterns to determine the upper bound of candidate faulty cells and test patterns are the original test patterns which are used to test the CUT. After the logic simulation, we obtain the simulation responses which are not affected by the faulty scan cell. By comparing the simulation responses and the faillog responses obtained from the ATE, we can derive the upper bound of the potentially faulty scan cells and the candidate scan cell window (CSCW) is defined as the range from 1st scan cell to the upper bound.

3. Post-process of the SF-Sym Diagnosis

As mentioned in Section 2, procedure (3) and (4) of the SF-sym, the post-process, are required to identify more exact candidate scan cells in the faulty scan chain. In third procedure of the overall SF-Sym algorithm, a new symbolic simulation for the scan chain diagnosis is performed with a logic ATPG pattern. In this symbolic simulation, we consider the effect of errors caused by scan shifting in the faulty scan chain. After the symbolic simulation (the SF-Simulation), by analyzing the simulated response for each candidate scan cell in both the faulty scan chain and the good scan chains, we can reduce the size of the candidate scan cell window and obtain the list of candidate scan cells. Repeating these simulation and analysis procedures until the list of candidate scan cells is converged, we can determine the candidate scan cells which are most likely to contain the real defects.

3.1. Symbolic Simulation for Scan Chain Diagnosis

To consider the effect of the faulty scan cell in the candidate scan cell window and to more exactly identify the location of the faulty scan cell using the information of good scan chains, a new symbolic simulation method, SF-simulation (Scan cell Fault simulation), is proposed for scan chain diagnosis. The SF-simulation differs from the conventional fault simulation, because it assumes that there are faults only in the scan chain and all the logics except the faulty scan chain are fault free. Therefore, for the SF-simulation, faults are inserted only to the scan cells in the candidate scan cell window and then fault free circuit C is simulated, while, for the conventional fault simulations, the fault free circuit C is transformed to the circuit C created by the logic fault f in the target fault lists and then the faulty circuit C is simulated. For the conventional fault simulations, it is very time consuming operation since the simulation time depends heavily on the number of target faults. However, for the proposed symbolic simulation, it is a very simple operation since the faulty scan chain model Sf is transformed to apply the effect of the faulty scan cell in the faulty scan chain, and just a single logic simulation is performed.

For the proposed symbolic simulation, in addition to the logic states \{0, 1, X\}, we introduce a new symbolic logic state SF, which means the location of fault candidate scan cell, that is, the \(\alpha\)th scan cell in the faulty scan cell for considering the effect of faults in the faulty scan chain and for distinguishing the location of the faulty scan cell. Fig. 1 shows how to inject a new symbol into the faulty scan chain. Note that a test pattern included in the new symbolic logic states SF, is called an SF pattern.

![Figure 1. An example of the SF pattern](image-url)
In Fig. 1, if a test pattern applied after the calculation of the candidate scan cell window is \(011010001\), then the actually loaded test pattern to the faulty scan chain may be \(011011111\). It is clear that the test response for the loaded scan-in pattern is different from the simulation response of the original test pattern which does not consider the effect of the faulty scan cell \(SC_a\). Therefore, there are significant mismatches between the simulation result and the unloaded test response in the faulty scan chain as well as in good scan chain. It diminishes the precision of the scan chain diagnosis. To alleviate this problem, new states, \(SF_i \sim SF_e\), are injected to the candidate scan cells in the candidate scan cell window. In addition, the test pattern values from \(SC_7\) to last scan cell \(SC_9\) are set to the faulty value since they are located after the candidate scan cell window and they are affected by the last faulty cell during the scan-in shifting. Therefore, the simulation results with the SF pattern are similar to the faillog response and the SF states can help to reduce the number of the fault candidates since some SF states can be propagated to scan-out responses of good scan chains or primary outputs. After injecting the SF states in the faulty scan chain, the logic simulation with the SF pattern is performed. For the logic simulation, we propose a heuristic method for three reasons: 1) to easily evaluate logic values, \(\{0, 1, X, SF\}\), 2) to reduce the memory size for the evaluation of the SF states and 3) to simplify the analysis to diagnose the faulty scan chain.

In general, a gate output value is determined by the controlling value if there is an input signal at a minimum, which has the controlling value. Otherwise, the gate is evaluated like a buffer or an inverter. Similarly, the specified value is propagated to the output of the gate when the input signal is a SF state and the input signal of the remaining input signals is a controlling value. If all the side input signals except one input which has a SF state have non-controlling value, the gate output value is determined by the value of the SF state. In addition, the output value is evaluated for the product of the SF state values if there are two SF input signals or more for any gate types. If the evaluation results of two SF input signals are propagated to the primary outputs or to the scan outputs as logical forms or CNF forms, such as \(SF_e \& SF_e\), then a big memory size would be required and the computation complexity to analyze the SF evaluation results propagated to the outputs would be enormously increased. Therefore, we use the product forms of the SF state values as the SF evaluation method. In addition, to reduce the complexity of the symbol computation, we do not use the inverting value, \(SF_i\).

Using this implementation method for the SF values with ATPG patterns, the original logic values, \(\{0, 1, X\}\) and the SF values can be propagated to the primary outputs and the scan cells and then the simulated output values can be stored as the SF response.

**Definition 5: (SF response)** The SF response of a scan chain is the value combination of SF-simulated outputs after the SF simulation with a SF pattern.

The proposed SF-simulation has a disadvantage. This simulation requires many symbols for SF values in the candidate scan cell window when the size of the candidate window is quite large. The worst case is when the upper bound is the last cell of the faulty scan chain. Since the usage of many symbols enlarges the calculation of symbolic simulation, it can make the symbolic simulation not so effective. To alleviate this problem, we use the binary or quartering division that is performed by ruling out half or quarter of the current candidate scan cell window at each SF-simulation. For binary division, as shown in Fig. 1, the candidate scan cell window is divided by half of its size and then the SF values and the don’t care values are injected into the foregoing part of the divided candidate scan cell window and the remaining part, respectively. After that the simulation responses of the 1st SF patterns are stored, the “X” values and the SF values are injected into the foregoing part and the remaining part, respectively. In this case, therefore, two SF-simulations are performed and two SF responses are stored per test pattern. These SF responses are used to determine the candidate scan cells by the diagnosis method described in the following subsection. Through the binary division during the SF-simulations, the calculation for the SF symbols can be reduced significantly.

### 3.2. Identification of Candidate Scan Cells

To identify the location of the faulty scan cell, three output responses must be compared: (1) simulation response set \(R_{\text{sim}}\), (2) faillog response set \(R_{\text{fail}}\) and (3) SF response set \(R_{\text{SF}}\). In this procedure, the output responses of the good scan chains should be used, while the information of the faulty scan chain is used in the procedure of generating candidate scan cell window.

As shown in Fig. 2, the faillog responses are different from the simulation responses in the faulty scan chain as well as the good scan chains because the faulty scan cell affects the scan-in pattern and then the effects of the faulty scan cell are propagated to both the faulty scan chain and the good scan chains. For example, in good scan chain 1 of Fig. 2, the simulation values of \(SC_0, SC_7\) and \(SC_9\) are contrary to real scan-out values.

**Definition 6: (Propagated Fault Effects)** The effects of the scan cell faults can be propagated to the faulty scan chain as well as the good scan chains. These effects are defined as the propagated fault effects (PFEs). Therefore, the good simulation responses of the good scan chains differ from both the snapshot responses and the faillog responses of them. Assuming that the circuit logics enclosed in scan chains are fault-free, the errors of these mismatch locations (PFEs) must be caused by the faulty scan cell.

Using the SF-simulation, the information of the candidate scan cells can be propagated to the primary outputs and scan chain outputs and these output values are stored as the SF response set \(R_{\text{SF}}\). Fig. 3 shows an example of the SF response set in the same case of Fig. 2.
Using the PFEs and the PSFs, we can reduce the list of candidate scan cells. Initially, the list of candidate scan cells is the same as the candidate scan cell window. The identification procedure of the fault candidates consists of the following steps.

1. Select a good scan chain.
2. Find locations of the propagated fault effects by comparing the simulation response set of the original test pattern, $R_{sim}$, and the faillog response set $R_{fail}$. Set these locations to $L_{fail,i}$ where $i$ is the index of the PFE scan cell.
3. Find locations and the SF states values of PSFs by analyzing the SF response set $R_{SF}$. Set their locations and symbolic values to $L_{SF,i}$ and $V_{SF,i}$ where $i$ is the index of the PSF scan cell, respectively.
4. Analyze the $L_{fail,i}$ and $L_{SF,i}$ and update the list of the candidate scan cells.

a) If the index of $L_{SF,i}$ and the index of $L_{fail,i}$ are matched, then the score of the candidate scan cell matched to $V_{SF,i}$ add 1.

b) If there exists only $L_{SF,i}$ among the $i$th scan cell responses, then the candidate scan cell matched to $V_{SF,i}$ is eliminated in the list of the candidate scan cells.

c) If there exists only $L_{fail,i}$ among the $i$th scan cell responses and the value of $i$th scan cell in the fail response differs from the value of the same location in the SF response, then this can be one of two cases: 1) the product form of SF state values is exists in the same index of the SF response and 2) the combinational logic in the CUT is a faulty circuit. To reduce the complexity of the scan chain fault diagnosis, these situations are ignored in our proposed method.

d) If there exists only $L_{fail,i}$ among the $i$th scan cell responses and the value of $i$th scan cell in the fail response is the same as the value of the same location in the SF response, then this can be ignored since this faulty value is affected by the faulty pattern value behind the candidate scan cell window.

(5) Repeat step (1)-(4) for all the good scan chains.

By iterating step (1)-(5), we can reduce an increasingly greater number of the candidate scan cells, updating an increasingly smaller size of the candidate list. The proposed scan chain diagnosis procedures are repeated until the list of the candidate scan cells is converged or the repeated count reaches the user-defined scan diagnosis limit $D_{lim}$.

4. Consideration of Multiple Faults

In the case of multiple faults in a single scan chain, the diagnosis resolution depends heavily on the types of faults in the scan chain. In addition, some faults in a scan chain are masked by the last fault in the same scan chain during scan-out shifting in the faulty scan chain. For example, if there is a stuck-at 0 fault in the last scan cell of the faulty scan chain, the unloaded scan output responses beyond the stuck-at 0
faulty scan cell are all 0s regardless of the fault types of previous faulty scan cells. Since many previous scan chain diagnosis methods suffered from these problems, they only have limited the ability of their scan chain diagnosis technique. Similarly, it is clear that the diagnosis resolution of our proposed SF-Sym diagnosis method also has a cope with these same problems. Therefore, modifications are necessary to each step of the proposed method.

For multiple faults in a single scan chain, in the flush test, the fault type cannot be identified exactly, because various faults in a single scan chain are affected each other and the effects of the faults are masked. In addition, for the generation procedure of the candidate scan cell window, the accuracy of the candidate scan cell window is not guaranteed because of ambiguous fault type of last scan cell. Therefore, the pre-process of the proposed SF-Sym diagnosis are unnecessary for multiple faults in a same scan chain. Instead, more SF-simulations and identification procedures are required to increase the resolution of the SF-Sym diagnosis for multiple faults in a single scan chain.

Initially, the size of the candidate scan cell window for multiple faults is the same as the length of the faulty scan chain. In the SF-simulation, SF state values are injected into all scan cells in the candidate scan cell window since the fault types of the faulty scan cell are unknown. After generating the SF patterns, the SF-simulations with these patterns are performed. Since more SF state values are used than those of the SF-simulation for single fault, the proposed scan chain diagnosis for multiple faults in a single scan chain can be more difficult and more test patterns are required to achieve a high diagnosis resolution.

Therefore, to improve the ability of the scan chain diagnosis for multiple faults, the proposed method adds a matching algorithm for the propagated fault effects and the propagated SF values. The locations of the PFEs, $L_{fail}$ are compared against the locations of the PSFs, $L_{SF}$. Based on a matching algorithm, a score is calculated and assigned to each candidate scan cell in the candidate list. The candidates are ranked in the decreasing order of scores with a higher score denoting a higher probability that the candidate is the actual defect site.

The proposed score matching method is based on the hypothesis that the more exact matching between the fault site and the actual defect site, the better matching between the locations of the PFEs and the locations of the PSFs. The calculation of the score is based on the following metric equation.

$$\text{Score}_{SF} = \sum_{j \in \text{good scan chain}} \left( \frac{NSF \times N_{\text{match}}}{N_{\text{good, sc}}} \right) + L_{\text{fail, sc}}$$

where $NSF$ is the number of the matched SFs in $L_{\text{fail}}$, which appeared as errors in the locations of the propagated fault effects, $N_{\text{match}}$ is the number of the matched scan cells in $L_{\text{fail}}$, and $N_{\text{good, sc}}$ is the number of total scan cells in $j$th good scan chain. The $L_{\text{fail, sc}}$ is assigned to 1 if the $i$th scan cell in the faulty scan chain is the location of the propagated fault effect, otherwise, it is assigned to 0.

The score of each candidate scan cell consists of accumulated values of $\text{Score}_{SF}$ for all applied ATPG patterns. Therefore, $SF$ which has a higher score is a much higher probability indicating that the candidate is the actual defect site. Using this score matching method, multiple fault sites in a single scan chain can be easily identified, but the exact fault type of each fault candidate cannot be determined.

5. Experimental Results

To determine the effectiveness of the SF-Sym diagnosis method, experiments were performed on ISCAS '89 and ITC '99 benchmark circuits of various sizes. A commercial tool that supports the scan chain insertion was used and an in-house tool that supports the combinational pattern generation was used as the ATPG engine. Note that scan chains for each circuit are inserted by using the commercial tool, the LBISTArchitect [12] in Mentor Graphics with the TSMC 0.25μm library. The proposed scan chain diagnosis method was implemented in C, and experiments were performed on a Blade 2000 system.

### Table 1. Comparison of diagnosis resolutions for a single fault (average)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>s5378</td>
<td>10</td>
<td>23</td>
<td>5.9</td>
<td>1.2</td>
<td>1</td>
<td>1</td>
<td>&lt;1</td>
</tr>
<tr>
<td>e9234</td>
<td>10</td>
<td>25</td>
<td>5.8</td>
<td>1.3</td>
<td>1</td>
<td>1</td>
<td>4</td>
</tr>
<tr>
<td>s13207</td>
<td>10</td>
<td>79</td>
<td>15.4</td>
<td>1.6</td>
<td>1</td>
<td>1</td>
<td>13</td>
</tr>
<tr>
<td>s15850</td>
<td>10</td>
<td>69</td>
<td>7.2</td>
<td>1.3</td>
<td>1</td>
<td>1</td>
<td>16</td>
</tr>
<tr>
<td>s38417</td>
<td>10</td>
<td>175</td>
<td>14.5</td>
<td>1.2</td>
<td>1</td>
<td>1</td>
<td>24</td>
</tr>
<tr>
<td>s38584</td>
<td>10</td>
<td>173</td>
<td>11.7</td>
<td>1.5</td>
<td>1</td>
<td>1</td>
<td>21</td>
</tr>
<tr>
<td>s10</td>
<td>5</td>
<td>22</td>
<td>1.2</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1 &lt;1</td>
</tr>
<tr>
<td>s11</td>
<td>2</td>
<td>19</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1 &lt;1</td>
</tr>
<tr>
<td>s12</td>
<td>5</td>
<td>26</td>
<td>2.4</td>
<td>1.1</td>
<td>1</td>
<td>1</td>
<td>1 &lt;1</td>
</tr>
<tr>
<td>s13</td>
<td>5</td>
<td>13</td>
<td>3.5</td>
<td>1.3</td>
<td>1</td>
<td>1</td>
<td>1 &lt;1</td>
</tr>
<tr>
<td>s14</td>
<td>10</td>
<td>30</td>
<td>2.5</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>20</td>
</tr>
<tr>
<td>s15</td>
<td>10</td>
<td>52</td>
<td>7.6</td>
<td>1.6</td>
<td>1</td>
<td>1</td>
<td>19</td>
</tr>
</tbody>
</table>

First we evaluate the ability of the diagnosis for a single fault in a single scan chain. Table 1 shows the size of the candidate list and the diagnosis resolution of the proposed scan chain diagnosis against the previous methods [7]. For the benchmark circuits, we injected 100 randomly selected defects in scan chains and ran a simulation to obtain the fail log file. Table 1 shows the effectiveness of the SF-Sym diagnosis method for a single fault in a scan chain. Note that we set α to 5 in order to calculate the candidate scan cell window, DR (diagnosis resolution) is defined as the size of the candidate list and DA in Table 1 is the diagnosis accuracy which means the probability of a real defect in the generated candidate list.

Column 3 of Table 1 presents the number of scan cells in the longest scan chain, and columns 4 and 5 show the diagnosis resolution generated using the method of [7] and the proposed method, respectively. As shown in Table 1, for the SF-Sym diagnosis method, the number of candidate scan cells
is significantly reduced. The smallest diagnosis resolution corresponds to b10, b11 and b14 circuits with a value of 1 and the largest to the circuit s13207 and b15 with a value of 1.6. Although all the injected real defects for simulation can be found in the generated candidate lists, the size of the fault candidate list for the proposed method is smaller than half of that of [7]. In addition, for the proposed method, the number of scan cells with the highest rank is one or two and this highest ranked scan cell is the location of the real injected fault. Therefore, even for a single fault, the proposed method is proven to be a more attractive method than the previous ones. Since the probability of the faulty effect in the fault site to be propagated to output responses is increased in larger VLSI circuits, the effectiveness of the proposed method for a single fault has grown increasingly greater as the size of the circuit is increased.

Next, in our experiments for multiple faults in a scan chain, the randomly selected double faults in 100 are injected to compare the diagnostic abilities of the previous method [7] for multiple stuck-at faults. To improve the diagnosis resolution for double faults in a scan chain, we used the score matching method presented in Section 4. Note that the configurations of the scan chains in the benchmark circuits are the same as those in Table 1.

In Table 2, columns 4 and column 5 present the probability of injected double faults in the top 2 ranks of the candidate list. Similarly, columns 6 and column 7 present the probability of top 5 in the generated candidate list. The proposed scan chain diagnosis method generated smaller lists of the candidate scan cells in all the benchmark circuits. Only 0.11–0.875 times the candidate lists to find the exact defect location were necessary for the SF-Sym method as shown in Table 2.

<table>
<thead>
<tr>
<th>Circuits</th>
<th>DR [7]</th>
<th>DR [SF-Sym]</th>
<th>DA of top 2 [%]</th>
<th>DA of top 2 [SF-Sym]</th>
<th>DA of top 5 [%]</th>
<th>DA of top 5 [SF-Sym]</th>
<th>CPU time (sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>s5378</td>
<td>10.4</td>
<td>4.8</td>
<td>6.9</td>
<td>9.4</td>
<td>0.9</td>
<td>0.5</td>
<td>1</td>
</tr>
<tr>
<td>s9234</td>
<td>2.8</td>
<td>4.8</td>
<td>6.9</td>
<td>9.4</td>
<td>0.9</td>
<td>0.5</td>
<td>1</td>
</tr>
<tr>
<td>s13207</td>
<td>24.6</td>
<td>4.8</td>
<td>6.9</td>
<td>9.4</td>
<td>0.9</td>
<td>0.5</td>
<td>1</td>
</tr>
<tr>
<td>s15850</td>
<td>11.5</td>
<td>2.8</td>
<td>4.8</td>
<td>6.9</td>
<td>0.9</td>
<td>0.5</td>
<td>1</td>
</tr>
<tr>
<td>s58417</td>
<td>23.2</td>
<td>2.8</td>
<td>4.8</td>
<td>6.9</td>
<td>0.9</td>
<td>0.5</td>
<td>1</td>
</tr>
<tr>
<td>s68584</td>
<td>28.7</td>
<td>2.8</td>
<td>4.8</td>
<td>6.9</td>
<td>0.9</td>
<td>0.5</td>
<td>1</td>
</tr>
<tr>
<td>b10</td>
<td>2.4</td>
<td>2.8</td>
<td>4.8</td>
<td>6.9</td>
<td>0.9</td>
<td>0.5</td>
<td>1</td>
</tr>
<tr>
<td>b11</td>
<td>2.7</td>
<td>2.8</td>
<td>4.8</td>
<td>6.9</td>
<td>0.9</td>
<td>0.5</td>
<td>1</td>
</tr>
<tr>
<td>b12</td>
<td>2.8</td>
<td>2.8</td>
<td>4.8</td>
<td>6.9</td>
<td>0.9</td>
<td>0.5</td>
<td>1</td>
</tr>
<tr>
<td>b13</td>
<td>5.6</td>
<td>2.8</td>
<td>4.8</td>
<td>6.9</td>
<td>0.9</td>
<td>0.5</td>
<td>1</td>
</tr>
<tr>
<td>b14</td>
<td>12.7</td>
<td>2.8</td>
<td>4.8</td>
<td>6.9</td>
<td>0.9</td>
<td>0.5</td>
<td>1</td>
</tr>
<tr>
<td>b15</td>
<td>15.1</td>
<td>2.8</td>
<td>4.8</td>
<td>6.9</td>
<td>0.9</td>
<td>0.5</td>
<td>1</td>
</tr>
</tbody>
</table>

6. Conclusion

This paper presented a new technique that diagnoses single fault as well as multiple faults in scan chains. In this paper, we propose a new symbolic simulation based scan chain diagnosis method to solve the scan chain diagnosis resolution problem as well as the multiple faults problem. The proposed method uses a new symbolic simulation with the faulty probabilities of a set of candidate faulty scan cells in a bounded range and to analyze the effects caused by faulty scan cells in good scan chains. We use the faulty information in good scan chains that are not contaminated by the faults while unloading scan out responses. In addition, a new score matching method is proposed to effectively handle multiple faults and improve the diagnostic resolution by ranking the candidate scan cells in the candidate list.

Experimental results show that for most of the diagnosis cases the proposed method can achieve high diagnosis resolution and high diagnosis accuracy for all benchmark circuits. For a single fault as well as multiple faults in scan chains, the proposed method is an effective scan chain diagnosis method.

References