Dynamic voltage Drop induced Path Delay Analysis for STV and NTV Circuits during At-speed Scan Test

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Abstract— **The NTV circuit has been introduced as a new low power design concept, which increases energy efficiency significantly. However, delay sensitivity of the NTV circuit is a major challenge. In addition, this problem can be more critical during at-speed scan test because of the dynamic voltage drop issue. In this paper, we propose a comparison of dynamic voltage drop induced path delay between STV and NTV circuits during at-speed scan test. To the best knowledge of the authors, it is the first time to analyze the voltage drop induced path delay during the NTV circuit scan test. Experimental results show that the path delay increment of NTV is larger than that of STV although the dynamic voltage drop of NTV is smaller than that of STV.**

Keywords; near threshold voltage; dynamic voltage drop; at-speed scan test; path delay;

I. INTRODUCTION

Recent trends of various electronic devices become smaller such as internet of things (IOT), the energy efficiency of VLSI has become the most important issue. According to [1], supply voltage at near threshold voltage (NTV) region is the optimal range for the energy efficiency because operating frequency decreases linearly but power consumption is decreased exponentially. Nonetheless, it also brings the critical design challenge, which is the delay sensitivity. In the NTV region, the performance variation increases significantly compared to the super-near voltage (STV) region, and therefore, it is very important to handle the power supply noise (PSN) to mitigate the variation in the NTV circuit [2]. From this point of view, the delay sensitivity of NTV can be more serious during at-speed scan test. This is because test power is typically much higher than functional power and excessive voltage drop is still a major concern during at-speed scan test (e.g., yield loss) [3]. Hence, it is required to understand power, dynamic voltage drop, and voltage-drop induced path delay during NTV circuit scan test. For this purpose, this paper presents comparative analysis for STV and NTV circuit. The experimental results show that the path delay increment of NTV (~50%) is larger than that of STV (~5%) during launch-off cycle although test power and dynamic voltage drop of NTV is much smaller than that of STV.

II. EXPERIMENAL FLOW

To analysis the power, dynamic voltage drop, and voltage drop induced path delay, the automated experimental flow is implemented as described in Figure 1. In this experiment, ISCAS s38584 benchmark circuit is synthesized by two libraries (STV = 1.2V and NTV = 0.5V) with 10 scan chains. The operating frequency of STV is 250Mhz and that of NTV is 25 Mhz. It is noted that the NTV circuit frequency is typically smaller 10 times than STV [4]. And then they are placed and routed with 400x400um^2 core size. The power distribution network is designed with four virtual power/ground pads, a power ring and 2x2 power straps. Each layout design is described in Figure 2. After the layout design, transition delay fault (TDF) test patterns are generated by the ATPG tool. Using these patterns, the logic simulator is performed with *standard delay format* (SDF) and the switching information is stored in the *value change dump* (VCD) format. With these generated files, power, dynamic voltage drop and voltage drop induced path delay can be analyzed.

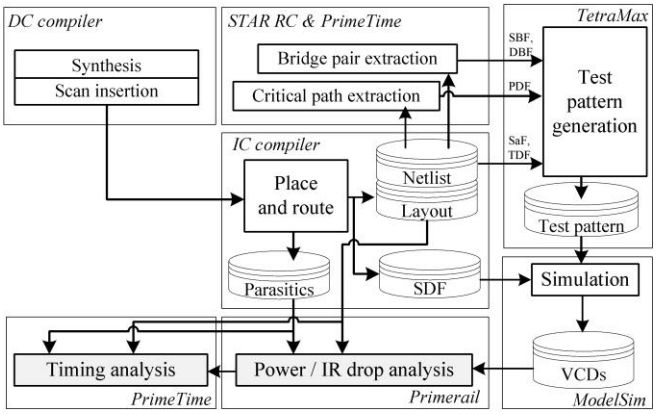

Fig. 1. Flow of the power, dynamic voltage drop and timing analysis

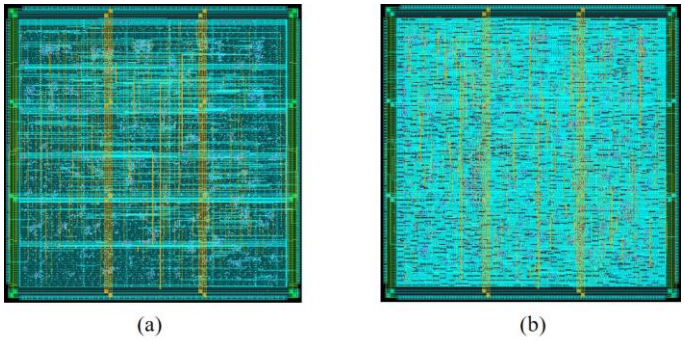

Fig. 2. Layout design of ISCAS s38584 using (a) STV library (b) NTV library

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TABLE I
COMPARATIVE ANALYSIS OF POWER AND DYNAMIC VOLTAGE DROP BETWEEN STV AND NTV ISCAS S38584 CIRCUITS

	Functional pattern (100 cycles, random patterns)				**TDF test pattern (launch cycle)**			
	Total cell power (mW)				**Total cell power (mW)**			
	TSP	TIP	TLP	TP	TSP	TIP	TLP	TP
STV(1.2v)	1.5257	3.4048	0.0013	4.9319	4.3720	9.7262	0.0015	14.0998
NTV(0.5v)	0.0277	0.0572	0.0012	0.0862	0.0619	0.0809	0.0010	0.1440
	VDD network				**VDD network**			
	Peak transient voltage (mV)		AVG transient voltage (mV)		Peak transient voltage (mV)		AVG transient voltage (mV)	
	MAX voltage drop		MAX voltage drop		MAX voltage drop		MAX voltage drop	
STV(1.2v)	81.892		8.725		110.594 (35%↑)		18.089 (107%↑)	
NTV(0.5v)	5.296		0.376		6.247 (17%↑)		0.526 (43%↑)	
	VSS network				**VSS network**			
	Peak transient voltage (mV)		AVG transient voltage (mV)		Peak transient voltage (mV)		AVG transient voltage (mV)	
	MAX voltage rise		MAX voltage rise		MAX voltage rise		MAX voltage rise	
STV(1.2v)	182.31		7.826		183.006 (0.5%↑)		16.198 (106%↑)	
NTV(0.5v)	7.138		0.299		7.571 (6%↑)		0.553 (84%↑)	

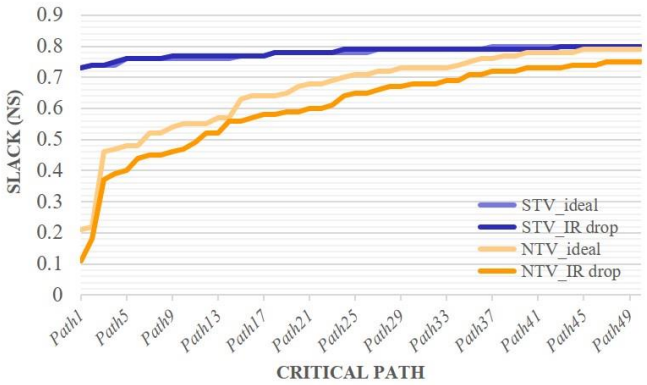

Fig. 3. Comparative analysis of ideal path delay and voltage drop induced path delay between STV and NTV ISCAS s38584 circuits

III. POWER, VOLTAGE DROP, PATH DELAY ANALYSIS

Table 1 shows the comparative analysis of power and dynamic voltage drop between STV and NTV circuits. First, a functional pattern is adapted to measure total cell power and voltage drop. Total switching power (TSP), total internal power (TIP), total leakage power (TLP) and total power (TP) are calculated in the STV and NTV circuit. Because dynamic power is strongly related to V_{DD}, total power of STV is much larger than that of NTV. During 100 cycles, dynamic voltage drop and voltage rise appears on VDD and VSS network because of the switching activity of each circuit. And then, a TDF pattern is adapted to compare to the functional pattern. In this case, the only one at speed launch cycle is observed because the excessive voltage drop issue during at speed scan test is typically related to this launch cycle [4]. The TDF test patterns of STV and NTV are same, and therefore, the total switching activity is almost same. Nonetheless, the rate of increase of total power, voltage drop and voltage rise is totally different between STV and NTV. Voltage drop of at speed scan testing in STV is larger than that of functional operation. However, in the NTV case, the rate of increase of voltage drop during at speed scan testing is around 43%. In addition to voltage rise on VSS network, the effect of PSN increment during at speed testing of NTV is much less than that of STV. However, the rate of increase of dynamic voltage drop induced path delay of NTV is much higher than that of STV as described in Figure 3. This timing analysis result is achieved among 50 critical paths using timing analysis. The maximum slack reduction rate is around 50% in NTV but it is almost under 5% in STV. Therefore, the delay sensitivity of NTV is still stringent compared to STV during at-speed test.

IV. DISCUSSION AND CONCLUSION

It is imperative to test NTV circuit to increase reliability and detect structural faults. In this paper, the automated experimental flow is introduced and the comparative analysis of power, voltage drop and path delay between STV and NTV. Although the PSN of NTV during at-speed scan test is much less than that of STV, the rate of increase of path delay of NTV is still larger than that of STV. This is because the delay of the NTV circuit is more sensitive. In addition, the power or timing margin of NTV is stricter than that of STV [5]. If the size of the benchmark circuit is very large (>100K gates), this trend is strongly exacerbated, and it can be concluded to yield loss or test cost increase. Therefore, the NTV-aware test methodology is strongly required to deal with this challenge.

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