Abstract—In this paper, a new repair scheme which consists of a new repair algorithm and a base die structure of TSV based 3D memory is proposed. The traditional repair process in 3D memory uses extra cells in each memory layer. This paper proposes a new redundancy cell structure for repairing memory layers using spare cells on the base die which consists of solution memory, spare CAM and a control structure. The experimental results show that the repair rate of the new repair scheme is better than that of the inter-die method.

Keywords—base die; post-bond repair; share cells;

I. INTRODUCTION

Memory technology has evolved to put lots of data on a small footprint. As the integration in the plane approaches technological limitation, 3D memory that stacks the integrated chips vertically has been developed. In 2D memory, reducing the area of the memory itself led to the increase in the degree of integration. However, in 3D memory in which where the memory layers are piled vertically, it is possible to increase the degree of integration not only by reducing the area, but also by building many layers.

If there are faulty cells in the memory, the entire memory must be replaced unless the cells are modified. As the degree of integration increases, it is economically disadvantageous for a company to discard a chip with a high price value due to minor failure. For this reason, testing memory chip failures has become significant, and the importance of repairing chips to achieve reasonable yield by putting redundant cells has increased. To solve these issues, papers such as SFCC [1] and Branch [2] have been presented.

There are two ways to repair 3D memory with extra cells. First, repair only the spare cells in each memory layer by using the 2D repair method. Second, if there are extra cells remaining, insufficient layer can get them from the other layers. The paper describing the second method is an inter-die [3] method.

This paper proposes a new 3D memory repair method that is more effective than the inter-die method using the free space of the logic base die of 3D memory. This method will be explained through operation algorithm, hardware structure for implementation, and comparative experiment.

II. PROPOSED IDEA

A. The Proposed Scheme

The proposed scheme consists of the algorithm and a new base die structure to realize the algorithm. The main idea is to put the spare cells for the post-bond which were put in each layer, on the base die. The structure is put in act like a cache, so it does logical substitution. The solution memory stores the repair solution from the repair process. Memory turned on, it sends the solutions to proposed spare structure. When a specific address is received for read or write operation, the control structure transfers the address to the spare structure and the memory layers. If spare structure has that address, it works read or write action. This spare cell structure should have the feature of searching for the address which it is carrying. So it can be called as spare CAM. Unlike previous repair approaches, this new scheme has no physical constraints like time delay when stacking many layers and increases availability of inter-layer spare sharing in post-bond situations.

B. Proposed Algorithm

Figure 1 (a) shows the repair process. After test each layer, presented fault information is analyzed to create a solution for each memory layer. This solution is stored in a non-volatile memory which called solution memory for future use. After proceeding with the test and saving the repair solution of all the memory layers, the repair process ends.

Figure 1 (b) shows the read/write operation process. When the power is turned on, the solution information of the solution memory is transferred to the spare CAM. In the case of writing, addresses and data are passed to the spare CAM and memory layers by the control structure. The CAM checks whether it has the address and then writes or ignores the data. In the case of a healthy cell, data will normally be put to the memory layer, and if it is a faulty cell, the data will be stored in the CAM as that it has an address. In the case of reading, address is also transferred from the control structure to the CAM and memory layers simultaneously. The CAM determines whether the address is a previously stored address. If the address is stored in it, the control structure selects data from CAM. If the address is not stored, the control structure selects and outputs the data from the memory layer. If the data of the healthy cell is required, the information of the memory layer must be sent.

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C. Proposed Base Die Structure

To implement the proposed scheme, spare CAM, solution memory, and a control structure are needed. The solution memory permanently stores the solution using the characteristics of non-volatility. This feature allows sending the data to the CAM when memory turns on. The spare CAM is installed to operate as a redundant cell upon receiving the repaired addresses. Finally, the control logic passes the incoming data and address to the CAM and memory layers, and determines what data to extract in the reading operation. This structure is shown in Figure 2.

III. EXPERIMENTAL RESULTS

The experiments were conducted to verify the performance of the proposed scheme. For the experiments, each memory layer has a 1024X1024 memory and post-bond repair is performed according to the various numbers of layers, spares and faults. For each case, 1,000 experiments are performed. Table 1 shows the repair rate comparison results with the fixed method and the inter-die method which can share spares between adjacent 2 layers. The reason for providing repair rate in Table 1 rather than normalized repair rate is that the proposed can repair some memories that cannot be repaired using other methods. The number of faults in Table 1 is the total number of layers in the memory layer and faults are distributed randomly in each layer. As a result, the number of layers increases, the repair rate differential between proposed and others becomes larger. The proposed can repair more memories than other approaches do and increase the memory yield.

IV. CONCLUSION

In this paper, a new repair scheme was proposed for 3D memory repair. It can be implemented by adding proposed structure to the base die of 3D memory. Compare with the two widely used methods in 3D memory repair, a remarkable increase in repair rate was noticed in the suggested algorithm. As the number of layers increased, this differential increased. However, it can be confirmed a big hardware due to the CAM size and long time for analysis compare to existing methods.

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REFERENCES


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Table 1. Repair rate of three 3D memory repair scheme