A TSV Test Structure for Simultaneously Detecting Resistive Open and Bridge Defects in 3D-ICs

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Abstract—After the 3D stacking process, TSV-based 3D-ICs are required to perform the post-bond testing in order to detect TSV faults or device functional defects. To detect the resistive open and bridge defects, various effective TSV testing techniques have been studied. At an early stage of TSV manufacturing, it is important to consider that the TSV testing is required not only determining whether each TSV is defective or non-defective, but also digitizing the fault degree into the TSV resistance value during the silicon debugging. In this paper, we propose a new TSV test structure for simultaneously detecting the resistive open and bridge defects with supporting the debug mode to analysis the characteristic of the specific TSV. It can highly reduce the test time by detecting TSV defects at the same time without compromising test quality.

Keywords; TSV test; 3D-ICs; resistive open and bridge defects; characteristic of TSV’s

I. INTRODUCTION

The device performance and functionality in 3D-ICs are highly impacted by the fidelity of signals through TSVs [1]. For this reason, the post-bond TSV testing is important to guarantee the quality and yield for mass production. The previous works [2, 3] are based on the voltage divider structure, which inspect the resistance-related delays by measuring the voltage across a TSV. These test methods can support to characterize the resistance of the defective or fault-free TSV for yield improvement during the silicon debugging and also to perform as a part of at-speed test to qualify timing specifications of 3D-ICs. However, the previous work [2] is only capable of testing the resistive open defects, which has inability to detect TSV-to-TSV bridge defects. In contrast to [2], the previous work [3] can detect both defects. It also provides lower hardware overhead and peak current consumption than [2] by using a shared comparator and a sequential pulse-transfer. However, the drawback of [3] is that each test for detecting the resistive open and bridge defects cannot be tested together at the same time. Each TSV testing needs the one test clock period per a single TSV, respectively. The total test time of [3] is $2 \times (\text{the number of TSVs}) \times \text{the test clock period}$. The proposed test structure is designed based on the previous work [3]; the voltage divider structure including a shared comparator and a sequential pulse-transfer. The proposed test structure can effectively reduce the total test time by using DFT (Design for Testability) techniques that provide the parallel test method without compromising test quality.

This work was supported by the National Research Foundation of Korea(NRF) grant funded by the Korea government(MISP) (No. 2015R1A2A1A13001751).

II. PROPOSED IDEA

A. Proposed Test Structure

The test structure of the previous work [3] consists of a shared comparator and a flip-flop to measure the voltage across a TSV ($V_{TSV}$), depending on the resistance of the TSV ($R_{TSV}$). Figure 1 represents the proposed test structure which adds a shared comparator, a XOR gate and a multiplexer in order to reduce the total test time in half, and it can be divided into three main parts. The first main parts consist of two shared comparators. The shared comparator compares two input voltage signals $V_{TSV}$ and $V_{REF}$. According to the experimental results of [3], the voltage level of the TSV-to-TSV bridge defects is greater than the standard voltage level of fault-free TSVs. In contrast, the voltage level of the resistive open defects is smaller. For this reason, the reference voltage ($V_{REF}$) of each shared comparator has the different value, and each upper and lower comparator is only capable of detecting the TSV-to-TSV bridge defects and the resistive open defects, respectively. The different $V_{REF}$ can be supplied by a single external pin, according to the voltage division rule. The second part is to determine whether the TSV has any defects or not. The outputs of each upper and lower comparator are supposed to be a logic 0 (low) and logic 1 (high) if $V_{TSV}$ is a fault-free value, as described in TABLE I. The final result is classified as a pass (1: High) or a fail (0: Low) by the XOR gate. Lastly, the third part is to select the test/debug mode by controlling the multiplexer. The default mode is the test mode (0: Low), but it can change to the debug mode (1: High) when it needs the fault diagnosis in detail whether the TSV defect is the resistive open defect or the TSV-to-TSV bridge defect. If the test/debug mode is changed from logic 0 to 1 right after the TSV is classified as a fail, the type of TSV defects can be diagnosed by the output
result of the next test cycle; the TSV-to-TSV bridge defect (1: High) and the resistive open defect (0: Low), respectively.

**B. Debug mode for analyzing the characteristic of TSVs**

Figure 2 shows the test flow diagram of the proposed test structure. The test flow of the normal mode is the same procedure as described in the previous subsection until it reaches the last TSV or the end of test. In addition, the proposed test structure can support the debug mode for analyzing the characteristic of a specified TSV by detecting the voltage across the TSV. To digitize the fault degree into the actual TSV resistance value, the voltage across a TSV can be measured by detecting the pass-to-fail or fail-to-pass transition point with sequentially increasing or decreasing the VREF value of the upper comparator. Consequently, the VTSV is the current VREF value at the transition point of the test result and it returns the end point value if there is no transition point. The VTSV value can be converted to the resistance of the TSV by HSPICE simulation results.

**III. EXPERIMENTAL RESULTS**

The proposed test structure is evaluated by using HSPICE (Nangate 45 nm Library). The representative value of TSV and FET specifications in the HSPICE simulation was extracted from published data [3]. Figure 3 shows the voltage profiles as a function of different RTSV and RBRIDGE. Each blue/red line represents the pass/fail condition, respectively. The VREF was determined by below test conditions. The TSV with the resistive open defect is presumed if the RTSV is greater than 500 Ω. In this case, the upper comparator output is staying the low regardless of the RTSV, but the lower comparator changes from high (Pass) to low (Fail) when the RBRIDGE is greater than 10kΩ.

The TSV is considered to be the bridge defect if the resistance between two TSVs is less than 10kΩ. In such a case, the upper comparator output switches from high (Fail) to low (Pass) when the RBRIDGE is greater than 10kΩ, but the lower comparator is staying the high regardless of the RBRIDGE. The outputs of both comparators transfer to the XOR gate which returns to the low if the TSV has any defects. In summary, experimental results guaranteed the test quality of the proposed test structure which can detect both the resistive open and bridge defects in parallel. Based on experimental results, the proposed test structure can reduce the total test time in half, compared to the previous work [3].

**IV. CONCLUSION**

In this paper, a new TSV test structure for detecting the resistive open and bridge defects and for supporting the debug mode is proposed. It can reduce the total test time in half with slightly increasing the hardware overhead, compared to the previous work [3]. Consequently, the test cost will dramatically decrease without compromising test quality.

**REFERENCES**

