A New In-field Bad Block Detection Scheme for NAND flash Chips

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Abstract— **a NAND flash system has been adopted as storage. However, due to its distinctive operation mechanisms, it endures only the limited number of program/Erase cycles. So, bad blocks are inevitably developed during the life time of the storage system. A bad block is a block that contains faulty bits that cannot be covered by ECC. In this paper, a novel in-field bad block detection scheme is proposed. Through simple write verifications, the proposed bad block detector finds bad blocks in real-time, and ensures that written data is reliable. The detection method includes neither costly data-mirroring nor complex ECC processing, but it requires an additional detection module of which size is less than 0.15% of the controller size.**

Keywords-component; NAND flash; Storage; Reliability;

I. INTRODUCTION

NAND flash chips have been deployed as data storage for various computing systems because of their nice features in term of low power, low cost, and high performance. However, NAND flash has limited Program/Erase (P/E) endurance, so that bad blocks are inevitably developed during the lifetime of the storage system. Bad blocks are blocks that contain one or more invalid bits whose reliability is not guaranteed. This problem is getting more exaggerated as high density NAND flash chips gain their momentum. For example, a multi-level cell NAND flash can endure only 5K P/E cycles while a single-level cell NAND flash endures 100K P/E cycles [1] [2].

Many researches have been done to solve this problem. Wear-leveling tries to balance P/E counts over different blocks so that all blocks may wear out at similar pace [3]. But this technique was developed without considering the difference in durability over blocks. So it is hard to say that bad block occurrences are sufficiently suppressed by the wear-leveling. So, ECC based bad block detection schemes are widely used at present [3]. In these methods, the ECC checks the validity of read data. If the read data is invalid, the block in which the data is stored is a bad block. The problem is that even if the ECC detected the bad block, the data written in the bad block is lost forever. To prevent this disaster, the corresponding data must be mirrored somewhere else in the NAND flash space [4].

In this paper, a novel in-field bad block detection scheme is proposed. Through simple write verification process, proposed Bad Block Detector (BBD) finds bad blocks in real-time without complex ECC process, and user data is protected without costly data-mirroring. By preventing user data to be written in a bad block, the proposed scheme enhances the reliability of the storage system.

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II. PROPOSED IDEA

The proposed BBD evaluates the reliability of blocks by comparing the last written data of each block with the corresponding golden data. The system architecture is shown in Figure 1, and it is described in *section A.*

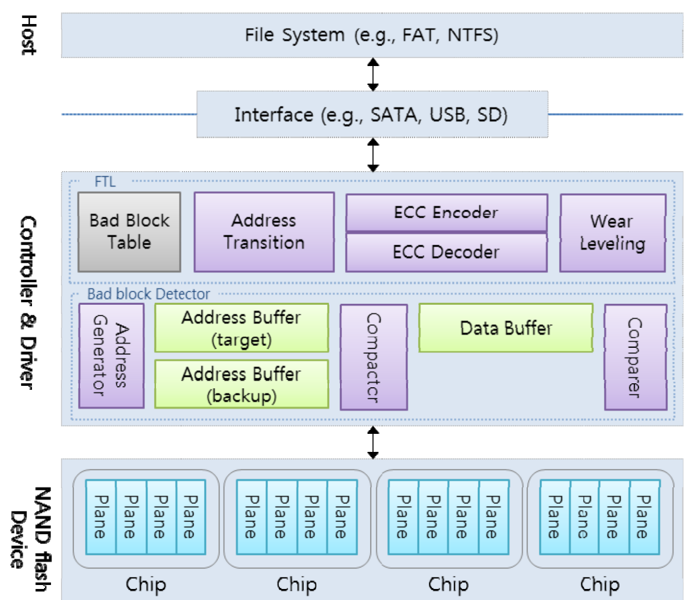

Figure 1. System architecture

A. System Architecture

The BBD is installed in the controller of the storage system, and it works as a middle layer between the FTL and the memory technology driver. The main role of the BBD is to determine whether the currently being programed block (target block) is a good block or a bad block. When a write request is issued from the file system, the FTL translates the Logical Sector Address (LSA) into a Physical Page Address (PPA) referencing the bad block table to avoid selecting a bad block. After, the data is written at the PPA location of a NAND flash chip, the BBD reads PPA location of the NAND flash chip, and compares the read data with the golden data stored in the Data Buffer to determine the reliability of the target block.

B. Bad Block Detector

In this section, the bad block detection process is described step-by-step, and an acceleration scheme is introduced. Figure 2 shows the architecture of the BBD.

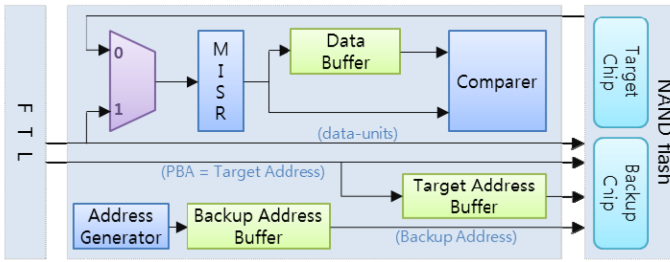

Figure 2. Bad Block Detector

The detection process can be divided into 3 steps. In step 1, the *PPA* is transmitted to the target chip, and it is stored in the target address buffer. The address generator selects backup chip from chips in idle state, and generates an address for the target chip (target address). In step 2, data-units are transmitted to both the target chip and the backup chip, and serially written from the PPA location of the target chip, and the backup-address location of backup chip. Meanwhile in the BBD, data-units are compacted through MISR, and the signature is stored in the data buffer. In step 3, BBD reads pages serially from the target address of the target chip, and compact them through the same process the data-units from the FTL are compacted. After the compaction is completed, BBD compares the signature in MISR with the value of Data Buffer. If they are not equal, the target block is a bad block. If so, FTL updates the Bad Block Table, and remap LBA to the Backup Address. Otherwise, BBD erases the backups because they are no longer needed. The detection latency is defined as equation (1).

$$L_D = T_R + (N_P - 1) * T_S + (N_P * T_{IO}) \quad (1)$$

L_D: detection latency N_P: number of page in write request T_{IO}: I/O time
T_R: NAND flash random read time T_S: NAND flash serial read time

In recent file systems, multiple data-units are programed serially in a single write request in most cases. For the NAND flash chip on the other hand, serial read is very simple task compared to random access [1]. So, the detection latency is not a critical factor for the write performance of the storage system.

C. *Copy verification*

Current NAND flash chips support copy-back operation in which a page is copied into another page in the same plane without transmitting the copy data to external components [1]. Since the BBD is a module in the controller, it cannot access to the copy data. So, the BBD verifies the copy destination block (DST) by comparing it with the copy source block (SRC) through the detection process described in *Section B*. In this case, the SRC is the golden data, and the DST is the target. If the DST block is found to be a bad block, the SRC is copied into Backup Address block again, and the FTL updates corresponding entry of its address mapping table.

III. Experimental Results

In this section, experiments are conducted to evaluate the performance of the proposed bad block detection scheme. The storage system is composed of 4 chips of K9GAG08U0M NAND flash, and an ARM based control unit. Under the same workload of real world file systems, ECC based bad block detection [4] and the proposed detection are compared in term of available user capacity, R/W performance, and the reliability of the data stored in the NAND flash. Table 1 shows the results.

TABLE I. Performance Comparison

Test Data	FAT32		EXT4		Multimedia Copy	
Detection Scheme	ECC Based	Proposed	ECC Based	Proposed	ECC Based	Proposed
CAP (MB)	3891	7782	3891	7780	3891	7068
RES (us)	407.23	428.48	534.89	566.53	797.52	803.07
RATE (%)	90%	100%	90%	100%	90%	95%

CAP: user capacity RES: average response time RATE: detection rate ratio

The proposed scheme does not include costly data-mirroring, so it provides 94% more user space. The ECC based scheme shows lower detection rate because ECC has its own limitation of error detection. For example, parity code cannot detect even number of bit error. Additional detection process of proposed one does affect the write performance, but it is negligible compared to the NAND flash program time.

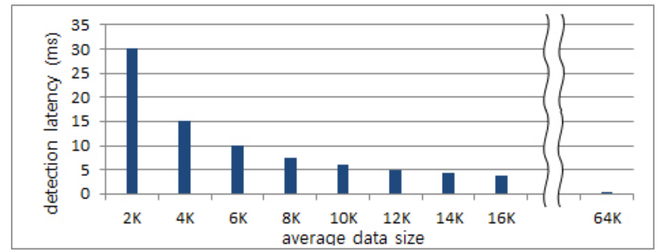

Figure 3. Bad block detection latency

In Figure 3, the detection latency following to the average data size for a write request is shown. For a workload in which sequential write operations are dominant, the performance degradation is negligible. Considering the detection rate and the available user space, this little overhead is worth to bear.

IV. Conclusion

In this paper, a new bad block detection scheme is proposed. The proposed BBD evaluates the reliability of blocks by verifying the last written data of each block. Through this method, bad blocks are efficiently detected in real time, so that costly data-mirroring is not needed. Experimental results show that proposed scheme provides twice as much user capacity compared to the conventional ECC based detection scheme, and it enhances the reliability of the storage system with negligible H/W overhead.

Acknowledgment

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