A Scan Segment Skip Technique for Low Power Test

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Abstract—**Excessive power consumption during testing has been one of the most important issues from the exponential advance in semiconductor manufacturing technology. In this paper, a scan segment skip technique is proposed to reduce power consumption by skipping segments that don't need scan in/out processes. Also, a new pattern merge algorithm is proposed for maximizing power reduction ratio. Experimental results show that the proposed technique efficiently reduces test power consumption with the minimal impact on area overhead.**

Keywords: scan-based test, test cost, test power reduction

INTRODUCTION

A scan architecture is a widely used methodology for the test very large scale integrated (VLSI) circuits. However, as the scan is used, a large power is dissipated during the test because of 1) Design-for-Testability (DFT) to reduce test complexity, not used in the functional mode but just used in the test mode, 2) lower correlation between test patterns in the test mode than that in the functional mode. Excessive power consumption can expose the circuit to various problems, such as premature destruction, reduced reliability and increased product cost. Furthermore, using high clock frequency or multi scan architectures to reduce test time has brought the more increased power consumption during the test.

There are two kinds of power: shift power that is dissipated during the shift operation and capture power that is dissipated during the capture operation. In order to reduce the test power, various test structures have been proposed. Low power Illinois scan structure [1] has been proposed to reduce dynamic power consumption by reducing scan in switching activity where all the chains contain the same scan data. The reference chain is fed directly by the scan input, and all the remaining shared chains are fed either from the scan blocks in the same chain or from the scan blocks in the reference chain. Scan chain partitioning and scan hold structure [2] has been proposed to reduce power consumption by decreasing the moving distance of the first flip-flop toggling in the scan chain. If there are n partitions, the power consumption reduction rate becomes $1/n$ in this structure. But it has large hardware overhead by using additional buffers to support scan hold and a large controller that consists of a large mode shift register and two kinds of counters. Flip-flop swapping technique [3] has been proposed to reduce power consumption during the shift operation by reducing transitions in scan chains through using a swapping technique. However it has large area overhead and it needs a lot of time to analyze test patterns before starting the test.

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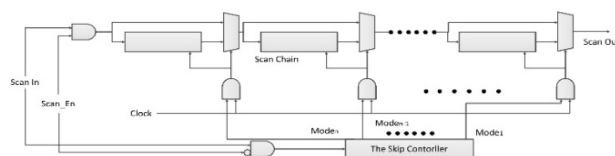

Fig. 1. The Proposed Structure with the skip controller

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A. The Proposed Technique

The proposed structure focuses on the shift power during the test. Some segments that don't need scan in/out processes during the shift operation are generated by the scan chain partitioning to reduce test power consumption or test time. The proposed structure can achieve test power reduction during the shift operation by skipping these segments, is shown in Figure 1. Each segment is activated by getting the clock signals that are gated with 'Mode' signals generated from the skip controller and can't be activated simultaneously by that just one 'Mode' signal can be set to '*1*' at a time.

If the number of partitions is n, there are $n+1$ states in the proposed structure. There is no skip segments during the shift operation in the state zero. The scan in/out processes are proceeded from the last segment to the first segment sequentially, and after a scan in/out process of the first segment, the capture operation is started. On the other hand, there is a skip segment in other states. The skip segment is different per states, the kth segment is skipped by that the '$Mode_k$' signal can't be set to '*1*' during the shift operation in the k state. The scan in/out processes are proceeded sequentially from the last segment to the first segment except for the kth segment in the k state.

B. Proposed Merge Algorithm

In order to support the proposed technique, a new test pattern merge algorithm is proposed to maximize test power reduction effect. The test patterns that have the same skip segment are grouped and merged in each group using a heuristic method with simulated annealing. If there are several segments that can be skipped in the patterns, the precedent segment that can be skipped is decided as a skip segment for grouping to maximize merge effects. After then, '*0*' is attached to all test patterns as the last bit except for the last test pattern in each group. The last pattern in each group has additional '*1*' as the last bit. As the proposed merge algorithm is used, effective test power reduction is achieved by generating many skip segments that can be skipped scan in/out processes.

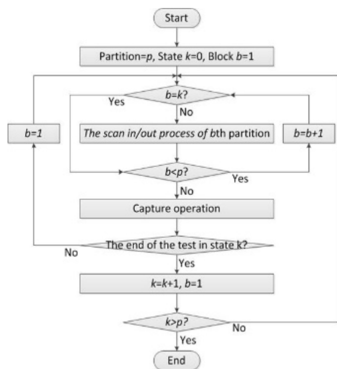

Fig. 2. Work Flow of the Proposed Structure

Furthermore, the ratio of remained don't care bits is a little large, it has effective power reduction as a proper low power X-filling technique is used.

C. *Work Flow of Proposed Technique*

The work flow is shown in Figure 2. Initially, the test that there is no skip process is done. After that, the skip controller receives a signal that represents the end of the test without skip process through scan in/out pins during the capture operation and as the state is changed, the test with skipping the first segment is performed according to the control signal of the skip controller. The skipping segment is changed sequentially from the first segment to the last segment whenever the skip controller receives signals that represent the end of the test with skipping each segment from the scan in/out pins during the capture operation. After the test with skipping the last segment is over, all the tests are finished.

EXPERIMENTAL RESULTS

Table 1 shows the experimental result using benchmark circuits. In order to calculate and analysis the average power, weighted transition count (WTC) and the number of cycles are measured. The average power is calculated as WTC divided by the number of cycles. In addition, the hardware overhead is measured to figure out the relationship between the number of partitions and the area overhead.

The second column shows the average power of the typical scan structure. And the last two columns show the average power reduction rate compared to the typical scan structure and the previous structure. As the number of partitions increases, the average power decreases. And the additional power reduction appears by the scan segment skip technique. Power reduction rate is up to 96% compared to the typical scan structure, 52% compared to the previous structure with the minimal area overhead except the B12 circuit. The area overhead of the B12 circuit is a little large because the small size of the B12 circuit have a great effect on area overhead.

In order to find the saturation point of the number of partitions, additional experiments are performed using the B20 circuit. As shown in Table 2, the average power is saturated when the scan chain are partitioned into 30 segments. If the number of partitions is larger than 30, the average power is changed without a regular variance. In addition, when the scan chain has been partitioned into 30 segments, the hardware overhead is measured about 2%. It means that there exists the optimized number of partitions and it can be mainly affected by the number of gates and the number of scan FFs in a chain.

CONCLUSION

In this paper, the scan segment skip technique is proposed to achieve test power reduction during the shift operation with the minimum area overhead. As mentioned earlier the proposed structure has effective power reduction. The scan segment skip technique has brought the additional power reduction effect by skipping several scan in/out processes with power reduction by partitioning. Furthermore, as the clock transition is reduced in clock tree by clock gating, the test power will be more reduced.

REFERENCES

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[3] Eman AlQuraishi & Reem AlTeenan, "Average Power Reduction in Compression-Based Scan Design", 15th IEEE Mediterranean Electrotechnical Conference, pp.504-509, April 2010

Circuit	Typical scan average power	The number of partitions	Previous Structure [2]				Proposed Structure				Red. (%) -Typ.-	Red. (%) - Pre.-
			WTC	The number of cycles	Average Power	Area Over. (%)	WTC	The number of cycles	Average Power	Area Over. (%)		
B12	18.334	5	28,618	5,642	5.07	23.64	18,926	4,537	4.17	9.18	77.26	17.76
		10	18,514	5,642	3.28	26.40	12,695	5,185	2.45	10.06	86.64	25.39
		15	14,912	5,642	2.64	27.72	9,900	5,380	1.84	12.50	90.00	30.38
B20	141	5	9,028,736	339,726	26.58	15.34	6,172,417	284,862	21.67	0.92	84.63	18.47
		10	4,761,198	339,726	14.01	15.55	4,553,641	428,598	10.62	1.15	92.47	24.19
		15	3,354,580	339,726	9.87	15.62	3,472,191	470,030	7.39	1.32	94.76	25.19
B22	178.591	5	29,423,638	874,530	33.65	7.29	15,345,500	559,125	27.45	0.76	84.63	18.43
		10	15,182,954	874,530	17.36	7.48	9,333,442	678,033	13.77	0.95	92.29	20.71
		15	10,780,296	874,530	12.33	7.60	6,605,371	730,176	9.05	1.13	94.93	26.61
B18	237.403	5	124,921,744	2,262,282	55.22	7.32	53,911,239	2,034,699	26.50	0.20	88.84	52.02
		10	62,370,634	2,262,282	27.57	7.37	31,332,905	2,293,330	13.66	0.25	94.25	50.44
		15	42,028,830	2,262,282	18.58	7.40	21,807,597	2,373,404	9.19	0.29	96.13	50.54

Table 1. WTC, cycle, average power and hardware overhead depending on circuits

B20	Typical scan average power	Previous Structure [2]				Proposed Structure				Red. (%) -Typ.-	Red. (%) - Pre.-
Partition		The number of partitions	WTC	The number of cycles	Average Power	The number of partitions	WTC	The number of cycles	Average Power		
26	141	1381	2,157,734	339,726	6.35	1444	1,505,215	341,997	4.40	96.88	30.70
28	141	1381	2,101,652	339,726	6.19	1446	1,440,975	343,707	4.19	97.03	32.23
30	141	1381	1,946,232	339,726	5.73	1441	1,328,855	342,853	3.88	97.25	32.34
32	141	1381	1,967,872	339,726	5.79	1445	1,485,670	345,040	4.31	96.94	25.67
34	141	1381	1,768,004	339,726	5.20	1444	1,207,028	345,011	3.50	97.52	32.78
36	141	1381	2,039,098	339,726	6.00	1446	1,614,086	346,605	4.66	96.70	22.41

Table 2. Experimental results of B20 circuit around saturation point