A NOVEL SCREEN-ABILITY ESTIMATION METHODOLOGY FOR DRAM WITH A TEST ALGORITHM SIMULATOR: FS5

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ABSTRACT

In commodity dynamic random access memories (DRAMs), many kinds of test algorithms are evaluated to guarantee the quality and the yield of mass production test processes such as wafer level test, package level test, and module level test. Traditionally, comparing the yield of each test process has been the only way to evaluate test algorithms' screen-ability for each test process. Some previous studies on fault-coverage of test algorithms have focused on only the sequences of test algorithms and data topologies. In this paper, a novel screen-ability estimation methodology is proposed and it estimates the screen-ability of test algorithms by calculating the probability of current leakages of some critical internal nodes and paths as well as the sequences of test algorithms and data topologies.

Index Terms— DRAM, test algorithm, simulation, SSI, MSSI, leakage path, screen-ability estimation

1. INTRODUCTION

As the progress of DRAM process technology, DRAM test algorithms become more complex. In addition, more elaborate cell layout schemes have been adopted such as $6F^2$ instead of $8F^2$ to increase the area efficiency of DRAM. In adopting $6F^2$ cell layout scheme, it becomes very important task to guarantee the same screen-abilities of test algorithms compared to those of traditional $8F^2$. From now on, screen-ability of test algorithms is estimated by the yield of each test process. But the estimation of test algorithms' screen-ability with yield of test process costs a lot of time and expense. So, it is indispensable to estimate the fault-coverage of test algorithms through different methods than real test process. There was an important study on the basics of theory and practice for testing memories [1]. Based on the concepts presented in this study, there have been some following studies on estimating fault-coverage of memory device [2-4]. They focused on mainly test sequences and data topologies regarding to test algorithms. However, there have been many kinds of test algorithms which developed to cover not only data topologies but also many internal current leakage paths around data storage nodes in DRAM mass production test. Because DRAM is containing data in it's capacitors at floating state, a slight leak current can cause the destruction of cell data. When the amount of leakage current is small, it is not enough to screen with focusing on only data topologies and the transition of the data. To accomplish the screen-ability even at those situations, considering the term of time is essential. And because there are many leakage paths other than cell-to-cell, it is also essential to take not only storage node but also other internal nodes into consideration. In this paper, screen-abilities of test algorithms are estimated by calculating the probabilities of current leakages through some critical internal leakage paths.

2. THE PROPOSED METHODOLOGY

In case of DRAM, data is recorded into a memory cell by storing or draining electric charge in storage node (SN). Normally, electrical nodes including storage node should be isolated against other nodes when they have different voltage levels. If there is a defect between any two nodes and voltage levels between them are different, the defect could become a leakage path and cause current leakage between the nodes. In this case, the total amount of moving electric charges is proportional to the product of the voltage difference and the time during holding this situation. For that reason, most of DRAM mass production test algorithms have been focusing on these leakage paths.

According to design layout and industrial experience, some important electrical nodes such as storage node (SN), substrate (Sub), cell plate (PL), word line (WL), and bit line (BL) have been tested in mass production as well as leakage paths between these electrical nodes such as SN-to-SN, SN-to-WL, etc. In order to estimate the screen-ability of test

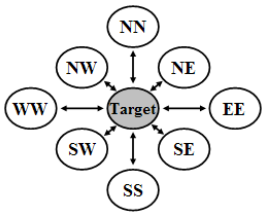

Figure 1: Arrangement of SNs

algorithms for these leakage paths, we developed a fault-coverage simulator called FS5 and have simulated screen-ability index (*SSI*) and Maximum *SSI* (*MSSI*) which are defined as follows.

$$SSI_{AB}(n) = Absolute\ \{V_{GAP}(n)\} \times T_{HOLD}(n) \quad (1)$$

$$MSSI_{AB} = Maximum\ \{\forall\, SSI_{AB}(n)\} \quad (2)$$

Where,

. V_{GAP} : $V_{Node\,A} - V_{Node\,B}$

. T_{HOLD} : Hold time during keeping V_{GAP}

The *SSI* in Equation (1) is calculated for all leakage paths. For example, there are 8 different *SSI*s on SN-to-SN leakage paths because a target SN is surrounded by 8 neighboring SNs as shown in Fig. 1. T_{HOLD} means the time during both nodes of a leakage path keep the same voltage difference. Generally, these electrical nodes are accessed several times according to the sequence of test algorithm during a test algorithm is running. The n in Equation (1), (2) represents n^{th} SSI_{AB} of a leakage path because SSI_{AB} has to be initialized to 0 in every access of the target node A or B. For this reason there would be many *SSI*s within a given test algorithm, so as to distinguish each *SSI* from others the n is used. Because the $MSSI_{AB}$ is the maximum value among the SSI_{AB}s, MSSI_{AB} can be inferred to represent the screen-ability of a test algorithm for the leakage path A and B.

3. A FAULT SIMULATOR: FS5

To evaluate the *MSSI* of test algorithms, we developed a fault-coverage simulator named FS5. FS5 consists of 5 functional modules which are condition extractor, algorithm converter, $8F^2$ analyzer, $6F^2$ analyzer, and result summarizer. The voltage and timing values of test algorithms are automatically extracted from the mass production test program by condition extractor module. Test algorithms need to be converted to pseudo algorithms because there are many types of test equipments in mass production test. The analyzer modules run pseudo algorithms and calculate *SSI* and *MSSI* of each test algorithm. The simulation results are collected by the result summarizer module. At the beginning of simulation, the analyzer sets target address using target information file and device information file. It also defines nodes and paths around the target address. After then the analyzer runs pseudo test algorithms. Each pseudo test pattern contains a series of DRAM command instructions, such as ACTIVE, READ, WRITE, PRECHARGE, etc. with address and data. Depending on what kind of command instruction is issued, which address is accessed and what data is given, voltage levels of nodes and their corresponding paths can be changed. The analyzer calculates V_{GAP} and T_{HOLD} for all pre-defined leakage paths in every clock cycles. Finally, when the running of pseudo test algorithm finishes, the analyzer calculates *MSSI* for all leakage paths.

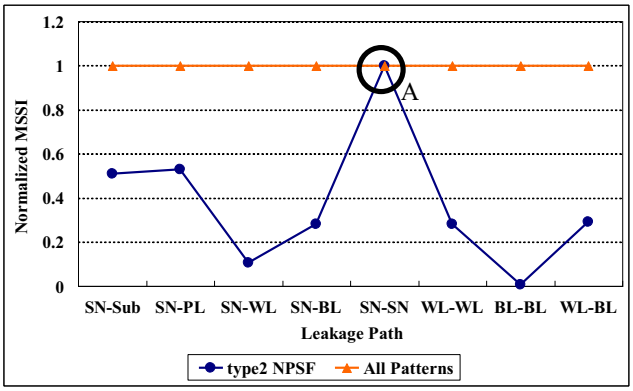

Figure 2: *MSSI* on All Leakage Paths

4. EXPERIMENTAL RESULTS

4.1. Screen-ability Estimation of type2 NPSF in DRAM

Most of previous studies' target memory is non volatile memory such as SRAM (static random access memory) and focused on cell topologies as well as data couplings around target cells [1]. However, as we have mentioned in section 2, DRAM requires refresh its cell data periodically unlike SRAM. So, many kinds of leakage paths weaken the retention time of DRAM and lead to fault. To guarantee the quality of commodity DRAM, the set of test algorithms must have screen-abilities for all the leakage paths. To evaluate the fault-coverage of test algorithms for DRAM, the simulator must inspect not only cell data and coupling between them but also other leakage paths. Figure 2 shows the difference of the normalized *MSSI* of tpye2 NPSF test algorithms and that of all test algorithms using in DRAM mass production test in Hynix semiconductor Inc. Type2 NPSF algorithm has been introduced in [1] and it is known as one of the most effective algorithms to detect coupling faults between target cells and their neighboring cells. This simulation results show that type2 NPSF test algorithm has good screen-ability for cell data coupling between them. SN-to-SN in Fig. 2 (i.e., 'A' in Fig. 2) represents this. However, the results also show that type2 NPSF test algorithm is not enough to screen all leakage paths in DRAM. For that reason, there are many kinds of test algorithms in DRAM mass production test to screen many leakage-oriented faults.

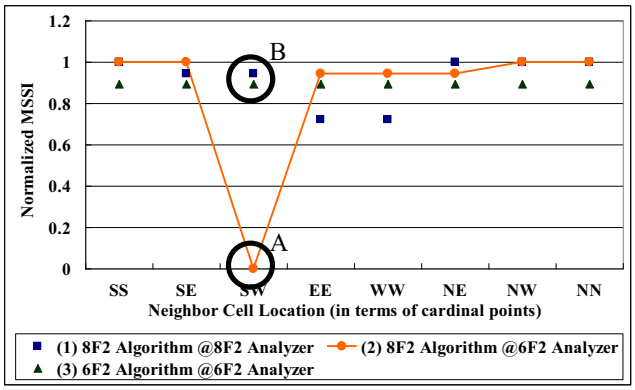

Figure 3: *MSSI* on SN-to-SN algorithm

4.2. Difference of SN-to-SN *MSSI* between $6F^2$ and $8F^2$

In light of the previous product development experiences, screen-abilities of test algorithms are comparatively well matched with the purpose of each test algorithm. To evaluate the precision of the proposed estimation methodology, three kinds of simulations were done; (1) $8F^2$ test algorithms with $8F^2$ analyzer, (2) $8F^2$ test algorithms with $6F^2$ analyzer, and (3) newly developed $6F^2$ test algorithm with $6F^2$ analyzer. Figure 3 shows the comparison of *MSSI* on SN-to-SN for a target SN against 8 surrounded neighbor SNs with three different simulations described above. As shown in Fig. 3, previous $8F^2$ test algorithms are not enough to cover $6F^2$ device if leakage current occurs between target SN and SW SN. Actually, the difference of BL structure between $6F^2$ and $8F^2$ devices caused this (see 'A' in Fig. 3). Although the case of SN-to-SN is not so difficult to understand, it is almost impossible to evaluate screen-abilities of all $6F^2$ test algorithms before real production without this simulator. As a result, a lot of $6F^2$-specific test algorithms have been developed based on results of this estimation methodology to compensate the lack of screen-ability (see 'B' in Fig. 3). They were inserted to the mass production test in Hynix semiconductor Inc. and almost same yields of $6F^2$ products in mass production test was achieved compared to that of $8F^2$ ones.

5. CONCLUSION

A novel screen-ability estimation methodology of test algorithms is proposed. In previous studies, only the sequence of test algorithms and data topologies are considered to estimated fault-coverage. However this methodology estimates the screen-ability of test algorithms by calculating the probability of current leakages of some critical internal nodes and paths. Furthermore, internal voltage levels and timings are considered in estimation as well as the sequence of test algorithms and data topologies. By using the proposed test algorithm simulator, identifying and improving screen-ability of test algorithms for DRAM mass production test is achieved before verifying it through expensive cyclic real production test.

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